PCI-104 Specification

Version 1.0

November 2003

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REVISION HISTORY

1.0, Nov, 2003

a. Formatted to meet the requirements of the PC/104 Embedded Consortium.

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1. INTRODUCTION

The ISA architecture bus has long been a popular choice for embedded applications. With the publication of the PC/104 standard in 1992, this bus architecture was available on a small, rugged form factor which has since become an industry standard. As technological requirements advanced, a need began to arise for a higher performance bus throughput. This is especially true when it comes to graphics devices as well as other high-speed I/O devices such as networks. The PC/104 Consortium met this challenge by incorporating a PCI bus on the PC/104 form factor, which became to be known as PC/104-*Plus*. This architecture provides a link to versatile legacy hardware while meeting the high-speed requirements for present and future hardware.

To accommodate the gradual replacement of ISA bus devices with PCI devices, the PCI-104 was approved by the PC/104 Consortium. PCI-104 is a PCI-only architecture that accommodates the advances of PCI devices in a small rugged form factor.

This document supplies the mechanical and electrical specifications for the "PCI-104" which has the advantage of the high-speed PCI bus.

1.1 Summary of Key Differences From PC/104 Specification:

- The AT and XT connectors for the ISA bus have been removed.
- The component height on the topside has been reduced from 0.435" to 0.345" and the bottom has been increased from 0.100" to 0.190" to increase the flexibility of the module.
- Control logic added to handle the requirements for the high-speed bus.

1.2 Summary of Key Differences From PC/104-*Plus* Specification:

- The AT and XT connectors for the ISA bus have been removed.

1.3 Summary of Key Differences (120-pin PCI and PCI Local Bus Specification)

- The PCI bus connector is a 4x30 (120-pin) 2mm pitch stack-through connector as opposed to the 124-pin edge connector on standard 32-bit PCI Local Bus.
- The 120-pin PCI does not support 64-bit Extensions, JTAG, PRSNT, or CLKRUN signals.

1.4 References

This document covers the addition of the PCI functions. The following documents should be used as reference for a detailed understanding of the overall system requirements:

- *PCI Local Bus Specification Revision 2.2*

Contact the PCI Special Interest Group office for the latest revision of the PCI specification:

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221
Phone: 503.291.2569 FAX: 503.297.1090
Email: administration@pcisig.com Website: http://www.pcisig.com

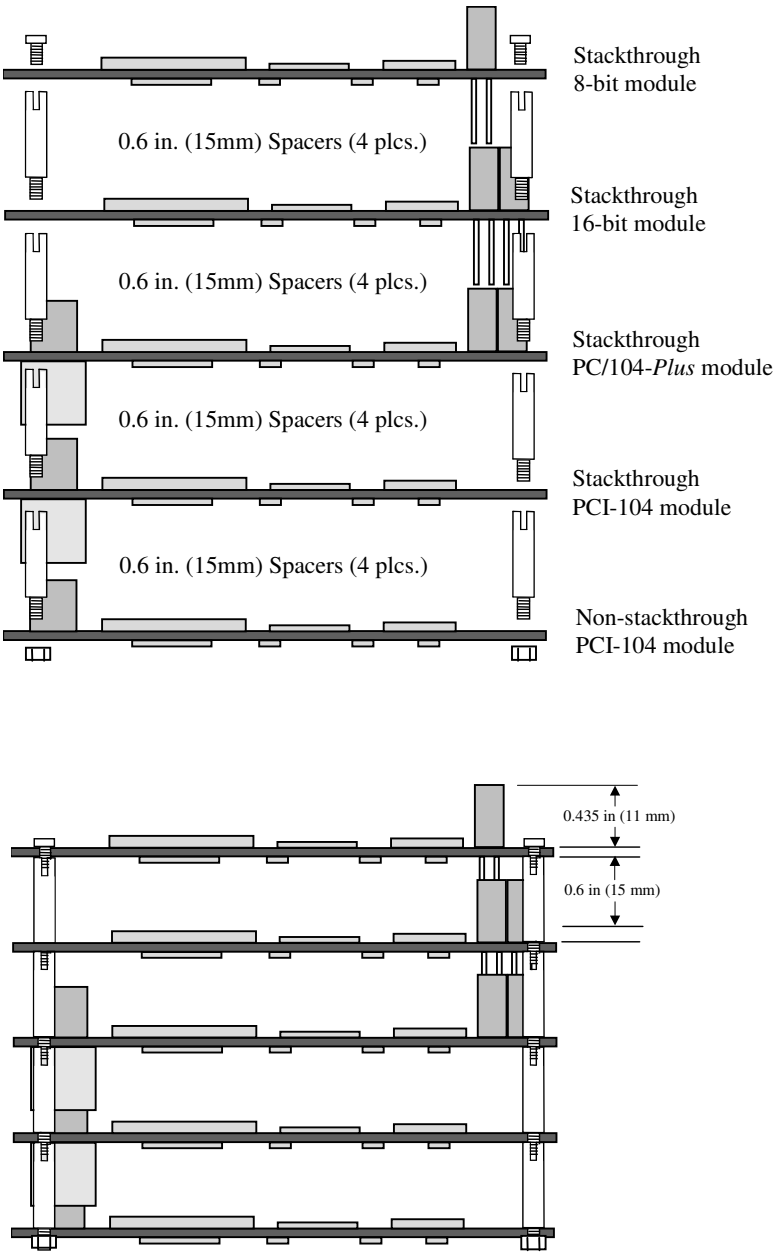
If errors are found in this document, please send a written copy of the suggested corrections to:

PC/104 Embedded Consortium
P.O. Box 78008
San Francisco, CA 94107-8008
Tel 415.243.2104 Fax 415.836.9094
E-mail info@pc104.org Website http://www.pc104.org

2. A POSSIBLE MODULE STACK CONFIGURATION

Figure 1 shows a typical module stack with two PCI-104 modules, one PC/104-*Plus* module, one PC/104 16-bit module, and one PC/104 8-bit module. The maximum configuration for the PCI bus of PC/104-*Plus* modules is four plus the Host Board. If standard PC/104 modules are used in the stack, they must be the top module(s) because they will normally not include the PCI bus.

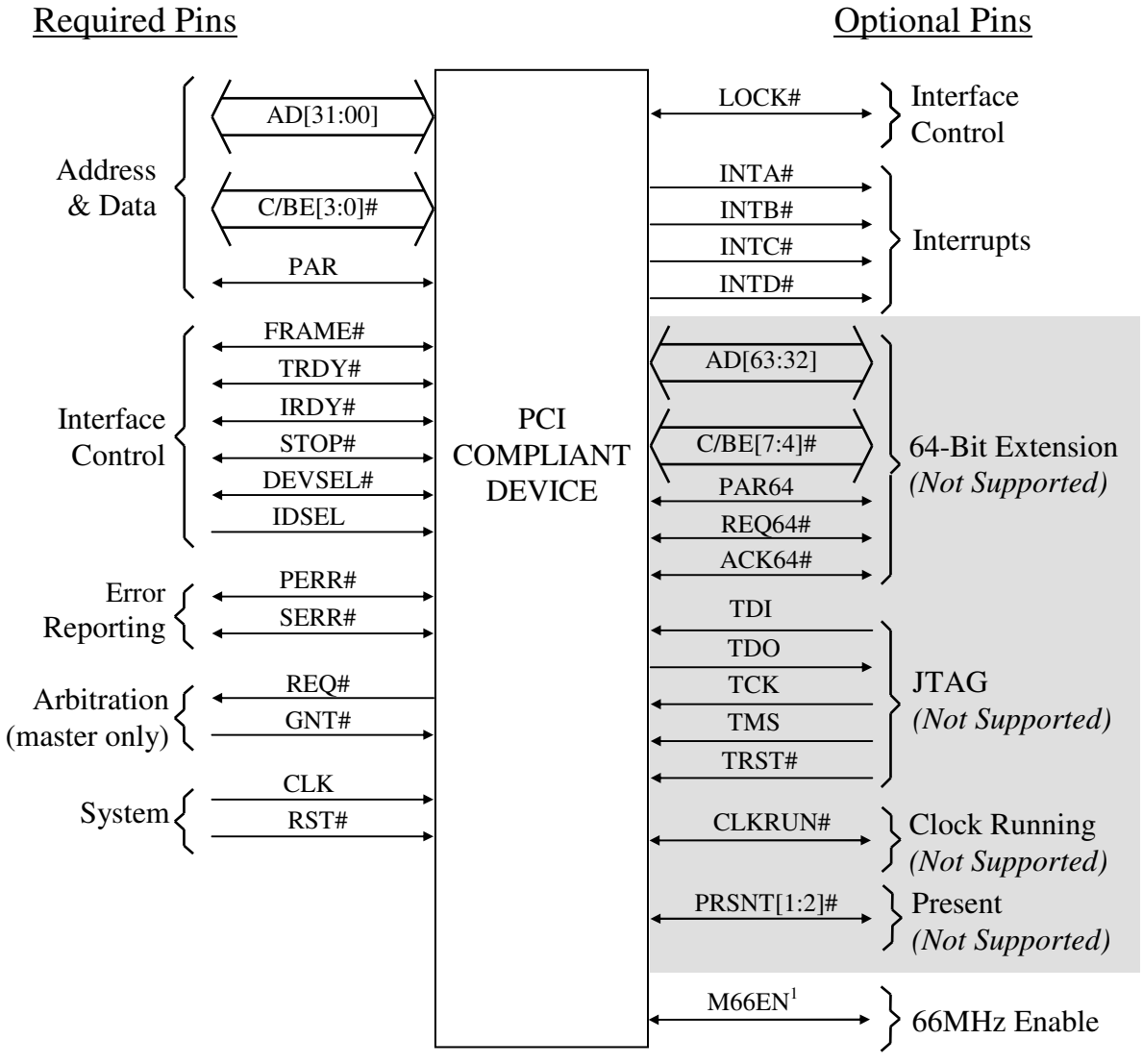
Figure 1: A Possible Module Stack Configuration



3. PCI SIGNAL DEFINITION

Figure 2 shows the pins in functional groups, with the required pins on the left and the optional pins on the right side. The shaded pins on the right are unsupported features, but are included to show the entire PCI bus as defined in the *PCI Local Bus Specification Revision 2.2*. This version of the PCI bus is intended as a 32-bit bus running at 33MHz and therefore, 64-bit extension and 66MHz[1] are not supported at this time. Also not supported are the boundary scan features (JTAG), *Present* (PRSNT[1:2]#), and *Clock running* (CLKRUN#). The direction indication on the pins assumes a combination master/target device.

Figure 2: PCI Pin List



[1] The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.

3.1 PCI Bus Signal Description

3.1.1 Address and Data

AD[31:00]	**Address and Data** are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases.
C/BE[3:0]#	**Bus Command/Byte Enables** are multiplexed. During the address phase of a transaction, they define the bus command. During the data phase, they are used as byte enables.
PAR	**Parity** is even parity across AD[31:00] and C/BE[3:0]#. Parity generation is required by all PCI signals.

3.1.2 Interface Control Pins

FRAME#	**Cycle Frame** is driven by the current master to indicate the beginning of an access and will remain active until the final data cycle.
TRDY#	**Target Ready** indicates the selected device's ability to complete the current data phase of the transaction. Both IRDY# and TRDY# must be asserted to terminate a data cycle.
IRDY#	**Initiator Ready** indicates the bus master's ability to complete the current data phase of the transaction.
STOP#	**Stop** indicates the current selected device is requesting the master to stop the current transaction.
DEVSEL#	**Device Select**, when actively driven, indicates the driving device has decoded its address as the target of the current access.
IDSEL	**Initialization Device Select** is used as a chip-select during configuration read and write transactions.
LOCK#	**Lock** indicates an atomic operation to a bridge that may require multiple transactions to complete.

3.1.3 Error Reporting

PERR#	**Parity Error** is for reporting data parity errors.
SERR#	**System Error** is for reporting address parity errors.

3.1.4 Arbitration (Bus Masters Only)

REQ#	**Request** indicates to the arbitrator that this device desires use of the bus.
GNT#	**Grant** indicates to the requesting device that access has been granted.

3.1.5 System

CLK	**Clock** provides timing for all transactions on the PCI bus and is an input to every PCI device.
RST#	**Reset** is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
M66EN	66 MHz Enable indicates to a device whether the bus segment is operating at 33 MHz or 66 MHz. The PCI bus has been simulated at 33MHz. For the purpose of this specification, 66MHz is not supported. To support future enhancements, the M66EN signal should be grounded on any module that cannot support 66MHz and left open for modules that can support a 66MHz clock.

3.1.6 Interrupts

INTA#	**Interrupt A** is used to request Interrupts.
INTB#	**Interrupt B** is used to request Interrupts.
INTC#	**Interrupt C** is used to request Interrupts.
INTD#	**Interrupt D** is used to request Interrupts.

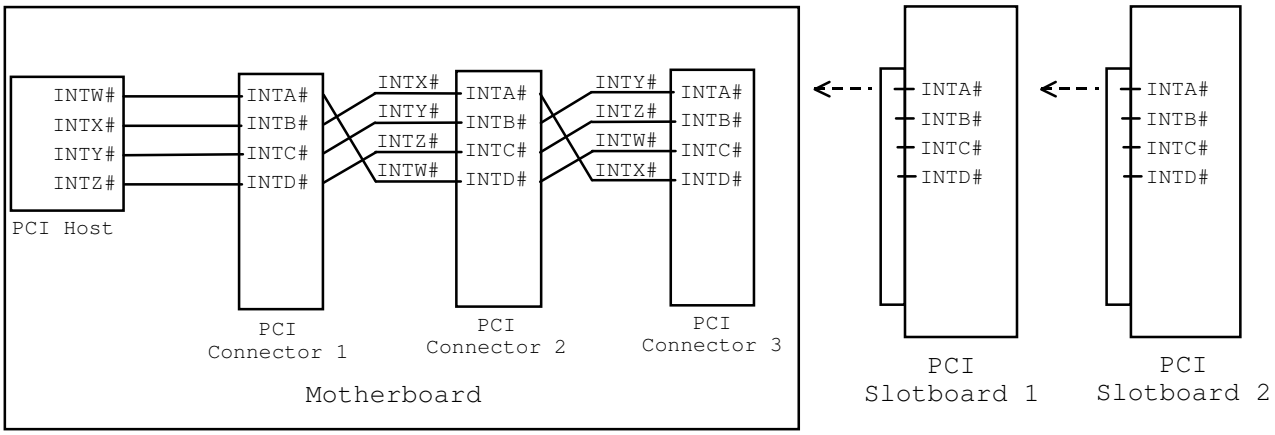
3.2 Signal Grouping

The PCI-104 architecture was developed to take advantage of the versatility and simplicity of the PC market for embedded applications. Like the desktop PC, PCI-104 has the ability to add auxiliary boards to expand the capabilities of the CPU. But instead of using slot cards, PCI-104 adds additional modules using stack-through connectors. This has two advantages: it reduces the system size and it makes the system more rugged so that it can better withstand shocks and vibrations.

To realize a stack-through architecture, a means of selecting the appropriate signals for each expansion card must be established that will easily allow for the installation and configuration of add-in PC/104-*Plus* and PCI-104 modules. The signals in question include CLKx, IDSELx, REQx#, GNTx#, and INTx# lines. Normal desktop computers overcome this problem by routing only the necessary signals to each of the slot connectors. For example, on a desktop PC, only CLK1, IDSEL1, REQ1#, and GNT1# are routed to PCI slot 1. Likewise, CLK2, IDSEL2, REQ2#, and GNT2# are routed to slot 2.

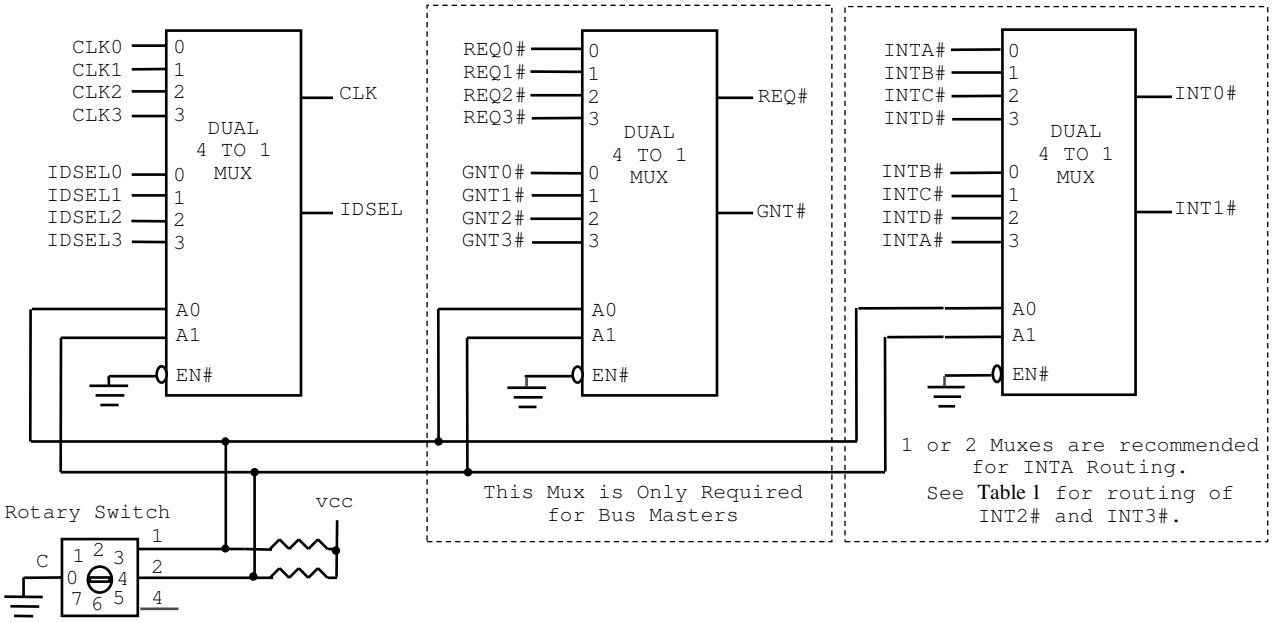
The interrupts on a desktop PC are handled in a different manner. All four interrupts from the interrupt controller are routed to each PCI slot connector. By convention INTA# on an expansion card is used for single-function devices and the remaining interrupts are used in the case of multi-functional devices. This could place a large burden on INTA# since all of the expansion cards would use this interrupt. To alleviate the burden, PC manufacturers stagger the interrupts on the motherboard to each of the PCI connectors. This is shown in Figure 3.

Figure 3: Interrupt routing for a desktop PC



Since PCI-104 is a stack-through architecture, there is only one connector to which all of the expansion boards must connect. A means of selecting the appropriate signals must be established that will easily allow for the installation and configuration of add-in PC/104-*Plus* and PCI-104 modules. Figure 4 shows such a method that can be applied to the expansion boards.

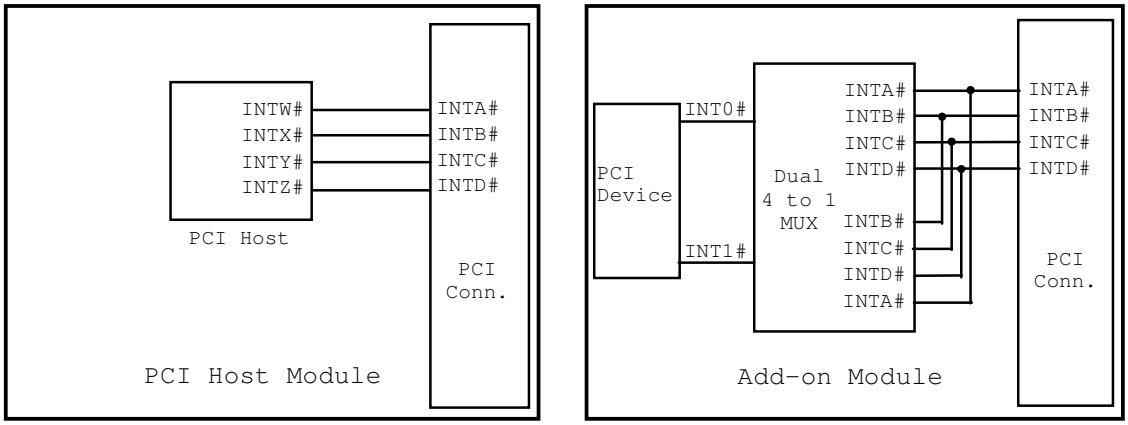
Figure 4: Signal Select on an Expansion Board



The multiplexer chips on the expansion board serve as the equivalent of having multiple PCI slot connectors on the motherboard of a desktop PC. To select the appropriate REQ#, GNT#, CLK, and INT signals for the expansion module, the rotary switch must be adjusted for the position on the stack.

For expansion modules requiring more than one interrupt, the staggering of the INTx# lines is accomplished on the expansion module prior to the multiplexers. Figure 5 shows the interrupt routing on a PCI Host Module and on an expansion module with two functions. The Add-on Module portion of Figure 5 shows how the right-hand multiplexer of Figure 4 fits onto an add-on module. If a board has a single function then only half of the multiplexer is required.

Figure 5: INT# Select



The multiplexer chips are Dual 4:1 Mux/Demux chips. They provide a 5Ω switch that connects the input and output together. These switches provide a bi-directional path with no signal propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. This is typically 250ps at 50pF load. Use one Mux for 1 to 2 interrupts or two Muxes for 3 to 4 interrupts.

While other methods of configuring the modules are possible and permissible, the rotary switch is clean and provides for the least possible error in configuration.

Table 1 shows the appropriate switch setting and signals used for each module in the stack.

Table 1: Rotary Switch Settings

Switch Position	Module Slot	REQ#	GNT#	CLK	INT0#	INT1#	INT2#	INT3#
0 or 4	1	REQ0#	GNT0#	CLK0	INTA#	INTB#	INTC#	INTD#
1 or 5	2	REQ1#	GNT1#	CLK1	INTB#	INTC#	INTD#	INTA#
2 or 6	3	REQ2#	GNT2#	CLK2	INTC#	INTD#	INTA#	INTB#
3 or 7	4	REQ3#	GNT3#	CLK3	INTD#	INTA#	INTB#	INTC#

4. ELECTRICAL SPECIFICATION

4.1 PCI Bus

The PCI Bus mechanical interface is a stackable 4x30 header. This interface carries all of the required PCI signals per *PCI Local Bus Specification Revision 2.2.*

4.1.1 Signal Definitions

For full details on the electrical requirements for the PCI bus, reference the *PCI Local Bus Specification Revision 2.2.*

4.1.2 Signal Assignments

Signals are assigned in the same relative order as in the *PCI Local Bus Specification Revision 2.2*, but transformed to the corresponding header connector pins. Because of the stack-through nature of the bus, slot-specific signals are duplicated for each plug-in module. The system has been designed to accommodate 4 modules, which are PC/104-*Plus*, PCI-104, or a combination of the two, so multiple sets of the signals have been duplicated to accommodate one signal for each module. These four signal groups include: IDSEL[3:0], CLK[3:0], REQ#[3:0], GNT#[3:0]. Signal assignments for the J3/P3 connector are given in Appendix B, Table 3: PCI Bus Signal Assignments.

4.1.3 Power and Ground Pins

The total number of power and ground signals remains the same, but the +3.3 V pins have been reduced by two and the ground pins have been increased by two. The change was the result of signal grouping on the bus and has no effect on performance or integrity.

4.1.4 AC/DC Signal Specifications

All bus timing and signal levels are identical to the *PCI Local Bus Specification Revision 2.2.*

4.2 Module Power Requirements

Table 2 specifies the voltage and maximum power requirements for each PCI-104 module. Care should be used in designing PCI-104 modules to guarantee the least possible power consumption. A worst-case module as specified could use almost 39 Watts of power, which would be unacceptable in most systems.

Table 2: Module Power Requirements

Supply	Min. Voltage	Max. Voltage	Max. Current	Max. Power
+3.3V	3.00	3.60	3A	10.8W
+5V	4.75	5.25	2A	10.5W
+12V	11.4	12.6	1A	12.6W
-5V	-5.25	-4.75	0.2A	1.05W
-12V	-12.6	-11.4	0.3A	3.78W

Note 1: Host Boards implementing "5 volt PCI signaling" are not required to supply 3.3 volts to the modules, but must provide a bus and decoupling. Host Boards implementing "3.3 volt PCI signaling" are not required to supply 5 volts to the modules, but must provide a bus and decoupling.

4.3 PCI Signaling Voltage (VI/O) Requirements

4.3.1 PCI Host Module

The PCI Host board will always determine the PCI signaling level on the bus by setting all VI/O pins to either 3.3V or 5V. If VI/O is set to 3.3V, then the system will use 3.3V I/O signaling and, likewise, if VI/O is set to 5V, then the system will use 5V I/O signaling. Some PCI host modules may only allow one of the options, while others may provide a jumper to allow the user to select the signaling level. Once the signaling level is selected, the remaining boards in the system must use that signaling level.

4.3.2 Add-In Modules

Add-in cards can be 3.3V, 5V, or universal.

3.3V Add-In Modules
3.3V add-in cards can only operate in environments where VI/O has been set to 3.3V by the PCI Host module. Using 5V add-in modules on a 3.3V stack will result in the 3.3V modules being damaged.

5V Add-In Modules
5V add-in cards operate in environments where VI/O has been set to 5V by the PCI Host module. Using 3.3V add-in modules on a 5V stack will result in the 3.3V modules being damaged.

Universal Add-In Modules
Universal add-in board can be used on either 3V or 5V I/O signaling buses. Universal boards either use the VI/O signal to determine its signaling level or are 3V signaling boards that have 5V-tolerant I/O. Many PCI interface chips have a "VI/O" pin that is the power for the I/O buffers that can be directly connected to VI/O. Universal boards will work on either 3V or 5V I/O signaling buses.

5. LEVELS OF CONFORMANCE

This section provides terminology intended to assist manufacturers and users of PCI-104 bus-compatible products in defining and specifying conformance with the PCI-104 Specification.

5.1 PCI-104 "Compliant"

This refers to "PCI-104 form-factor" devices that conform to all non-optional aspects of the PCI-104 Specification, including both *mechanical* and *electrical* specifications.

5.2 PCI-104 "Bus-compatible"

This refers to devices, which are not "PCI-104 form-factor" (i.e., do not comply with the module dimensions of the PCI-104 Specification), but provide male or female PCI-104 bus connectors that meet both the *mechanical* and *electrical* specifications provided for the PCI-104 bus connectors.

6. MECHANICAL SPECIFICATION

6.1 Clock Trace Lengths

The clocks are tuned on the Host Board such that the length of CLK3 trace is ≈0.662" less than CLK2, CLK2 trace is ≈0.662" less than CLK1, and CLK1 trace is ≈0.662" less than CLK0. Therefore, the first module on the stack must select CLK0 (the longest trace), the second CLK1, etc. This provides almost no clock skew between modules. Trace length limits are as indicated in the *PCI Local Bus Specification Revision 2.2*.

6.2 Module Dimensions

The mechanical dimensions for this module are identical to PC/104-*Plus* Specification with the exception of the removed ISA connectors and some modifications to the I/O connector area. The component height on the topside is 0.345" and the bottom side is 0.190". Exceptions to this are the regions along the sides of the module (indicated by the dotted regions in Figure 6) which have height restrictions of 0.435” for the topside and 0.100” for the bottom side. The mechanical dimensions and restrictions are given in Appendix A, Figure 6: PCI-104 Module Dimensions.

6.3 Connector and Shroud

The connector for the PCI bus is a 4x30 (120-pin) 2mm pitch connector. The shroud should be installed on the bottom of the PC board when a stack-through connector is used. The mechanical dimensions and restrictions for the PCI connector are given in Appendix A, Figure 7: PCI Connector, and in Figure 8: PCI Connector Shroud. The shroud should be properly marked to identify the PCI signaling capability of the board (see Section 6.4 Board Identifier).

6.4 Board Identifier

Manufacturers of PCI-104 modules must clearly label, near or on the PCI connector the module’s PCI signaling capabilities. The label is to guarantee proper module installation. Depending on the type of board manufactured, the label will be one of the following:

3.3V only

5V only

Universal

APPENDIX A

MECHANICAL DIMENSIONS

Figure 6: PCI-104 Module Dimensions

Dimensions are in inches / (millimeters)

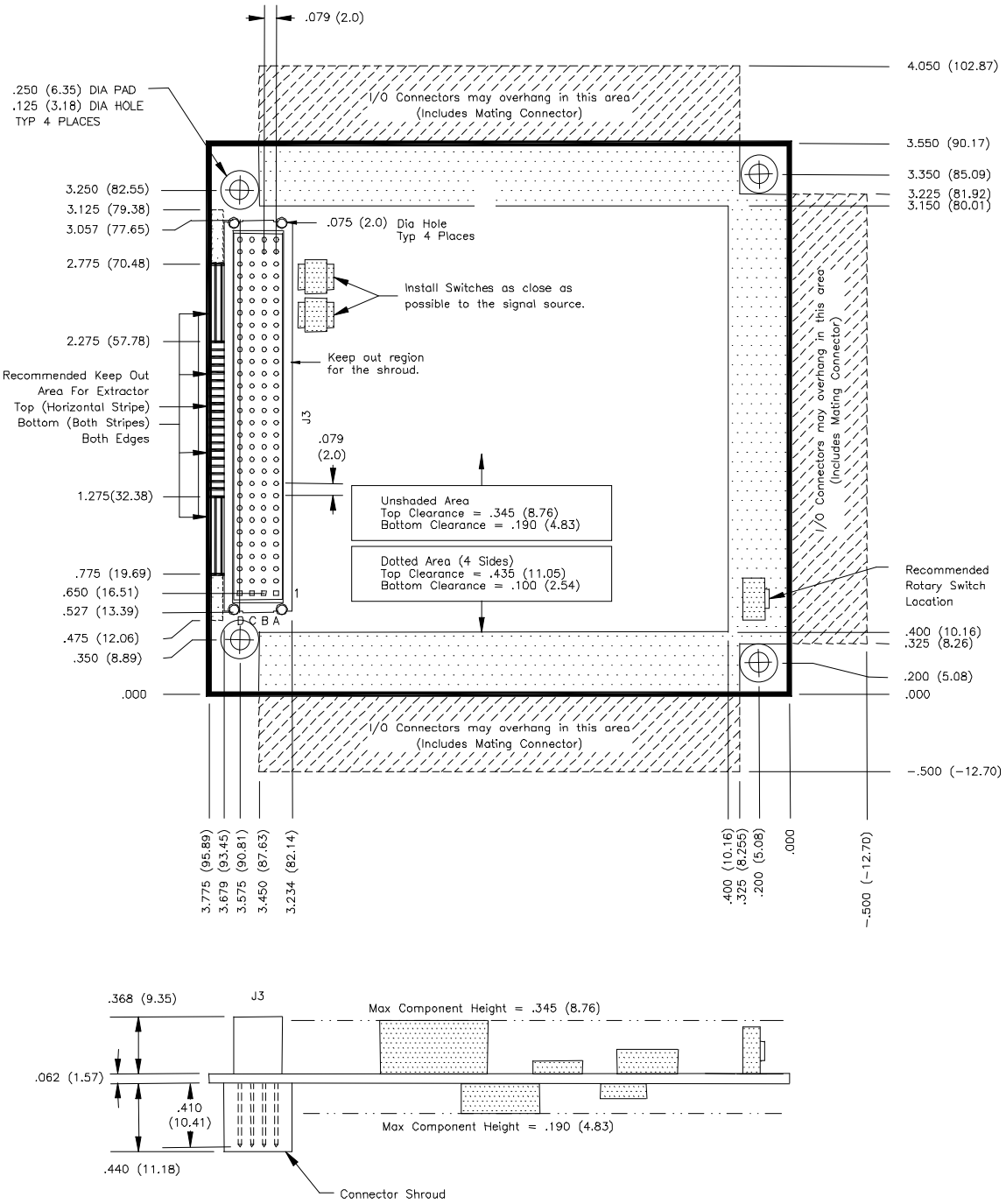


Figure 7: PCI Connector

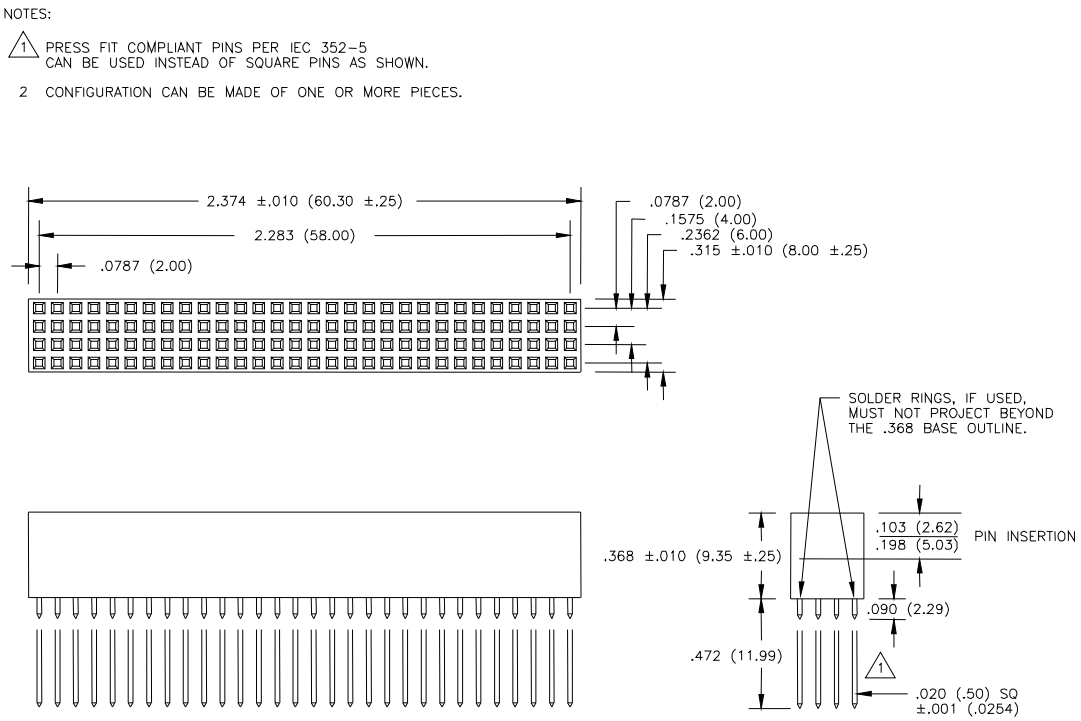


Figure 8: PCI Connector Shroud

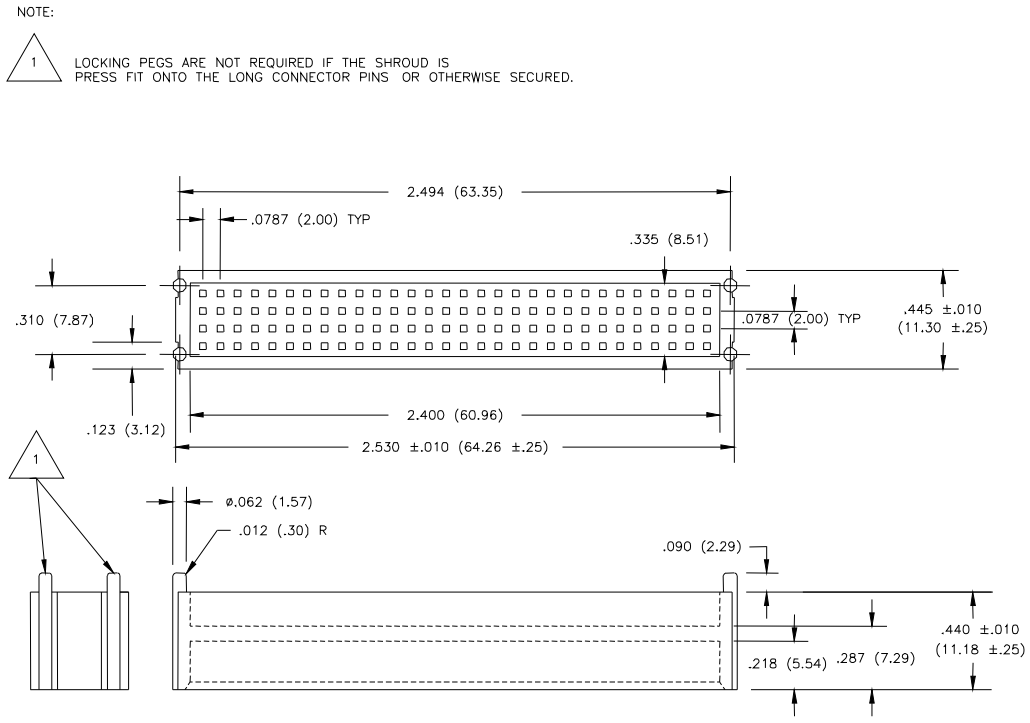


Figure 9: PCI Connector Specifications

Materials	
Housing:	High Temp Thermoplastic, UL Rated 94-V0
Contact:	Phosphor Bronze
Solder:	Tin-Lead (63-37), If Applicable
Solder Clip:	Aluminum Alloy, If Applicable
Contact Finish	
Female Interface:	15 Microinches Minimum Hard Gold
Male Interface:	Gold Flash Minimum
Solder Tail:	100 Microinches Minimum Solder
Underplate:	50 Microinches Minimum Nickel
Mechanical Performance	
Insertion Force:	2.5 Ounce Per Pin Maximum
Withdrawal Force:	1 Ounce Per Pin Minimum
Normal Force:	50 Grams Minimum (Per Beam)
Durability:	50 Cycles Minimum
Operating Temp:	-55° C To +85° C Minimum
Electrical Performance	
Contact Resistance:	<30 Milliohms Maximum
Current Capacity:	1 Amp Continuous Per Pin
Dielectric Strength:	500 Vac
Insulation Resistance:	5,000 Megohms Minimum

APPENDIX B

BUS SIGNAL ASSIGNMENTS

Table 3: PCI Bus Signal Assignments

J3/P3				
Pin	**A**	**B**	**C**	**D**
1	GND	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	Reserved	PAR
10	GND	PERR#	+3.3V	Reserved
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

Note: 1. The shaded area denotes power or ground signals.