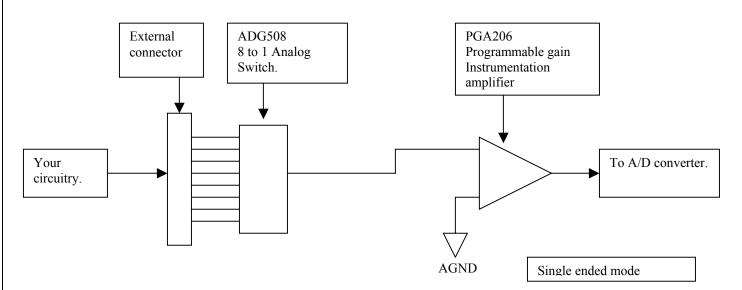
Analog Input Interfacing Considerations.

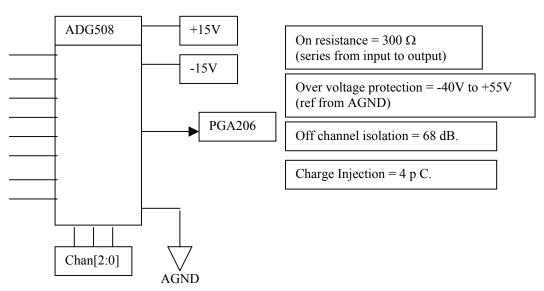
All of Diamond Systems analog inputs cards are basically the same so this document covers all of them. The DMM-32-AT, DMM-16-AT, DMM-AT, and PR-Z32-EA-ST are the most common.

Here is a simplified circuit diagram of the analog input stage.



The ADG508 and the PGA206 together play an important role to your interfacing circuitry.

The ADG508



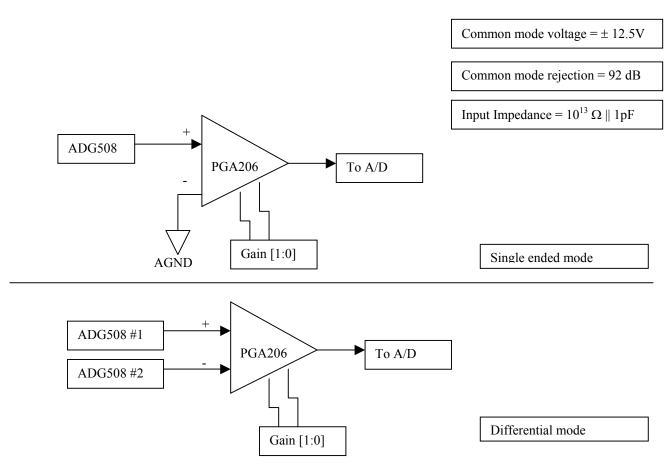
The 3 most important characteristics of the ADG508 are the over-voltage protection, charge injection, and the channel isolation.

Over voltage protection: Since this device is the very first component that your circuitry interfaces with you must be very careful not to exceed -40V to +55V referenced to our AGND. I state our internal AGND because if your interfacing circuit has a ground reference that is isolated from ours then it may be at a different potential. **Charge injection:** When the channels are switched this device will actually inject a charge into your circuitry. If you monitor one of the input lines with an oscilloscope you may notice a voltage spike during the channel change. This voltage spike will not interfere with the A/D reading as we switch channels at least 10uS before digitizing the input so it should have ample time to settle. The amplitude of this spike will increase if you increase the impedance

Diamond Systems Corporation 8430-D Central Ave. Newark, CA 94560 support@diamondsystems.com Author: Steve Hopkins, Systems & Support Engineer 8/20/04 of your interfacing circuits. Also a high impedance source may be affected by this charge injection as it may not be able to discharge the energy quickly enough.

Channel isolation: If you're worried about adjacent channel crosstalk then you should note that the isolation of this part is 68 dB and should not cause enough crosstalk to become an issue if your interfacing with a low Z circuit.

The PGA206



The 3 most important characteristics of the PGA206 are the common mode voltage, common mode rejection, and the input impedance.

Common mode voltage: This is the voltage measurement from AGND to the + and - inputs. These 2 inputs must be below ± 12.5 V otherwise the output will become unstable. Please be aware that if your interfacing circuits ground is not directly connected to our AGND then a potential between these grounds may be present which can cause the common mode voltage to be higher than expected which will cause instability in the sampled data.

Common mode rejection: This is the PGA206's ability to reject common mode noise. It is worthwhile to mention that once the common mode noise frequency is > 2 KHz then the parts ability to reject this noise drops logarithmically, which will cause instability in the outputs.

Input impedance: This device has very large input impedance so it is best to have very low output impedance on your interfacing circuitry.

Single ended vs. Differential mode

All of our boards have the capability to work in either mode. It is important to note that most interfacing problems occur in differential mode. The reason is quite simple because in differential mode it is easy to forget to provide a bias current path between your circuit and our AGND. When you are in single ended mode we internally connect the negative (–) side to AGND, which provides this path. See the data sheet page below for design considerations.

R1 adjusts the offset of the input amplifiers. Output stage offset is adjusted with R2. A buffer op amp is required in the output offset adjustment circuit, as shown, to assure that the Ref pin is driven by a low source impedance. To adjust for low offset voltage in all gains, first adjust the input stage offset in the highest gain. Then adjust the output stage offset (R_2) in G = 1. Iterate the adjustments for lowest offset in all gains.

Offset can also be adjusted under processor control with a D/A converter as shown in Figure 2. The D/A's output voltage can be reduced with a resistor divider for better adjustment resolution, but an op amp buffer following the divider is required to provide a low source impedance to the ref terminal. A different offset value is required for each amplifier gain.

INPUT BIAS CURRENT RETURN PATH

The FET inputs of the PGA206 and PGA207 provide extremely high input impedance. Still, a path must be provided for the bias current of each input. Figure 3 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the linear input voltage range and the input amplifiers will saturate.

If the differential source resistance is low, a bias current return path can be connected to only one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 3). These applications do not require additional resistor(s) for proper operation.

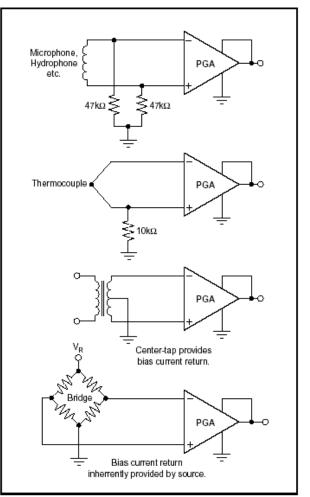


FIGURE 3. Providing an Input Bias Current Path.

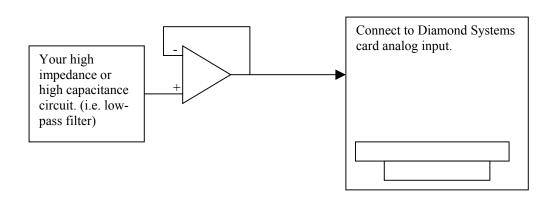
PGA206/207

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From Burr-Brown datasheet page 8.

The ideal circuit to interface with our analog inputs

Since the input impedance of the PGA206 is very high it is best to use a circuit with low output impedance. A unity gain op-amp like the OP4130 is a good choice to add as the last stage of your circuit if it has a high Z or high capacitance output.



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Guidelines for Interfacing

- Connect all unused analog inputs to AGND with short wires.
- Do not have long unterminated wires on any input.
- Only connect low Z outputs (< 200 ohms) to the analog inputs.
- When in differential mode try to always provide an input bias current return path and shown in the Burr-Brown data sheet above.

Known problems due to improper interfacing

You need extra delay time between input channel switching before sampling in order to get reliable data.

• This is a symptom of high Z circuits because it takes longer for our inputs to settle due to the charge injection from the analog mux.

You see large offsets or noise in your sampled (digitized) data.

• This could be a symptom of high Z interfacing or exceeding the common mode voltage.

Analog input switch damaged

• Typically caused by voltage spikes that exceed -40V to +55V. Remember this is referenced with our AGND so again if you ground is isolated from ours the risk of damage increases.

DC-DC converter damaged

• We have noticed that sometimes when the ADG506 analog input switches are damaged they occasionally short their ± 15V rails to ground. Unfortunately these DC-DC converters can't handle the short so they will sometimes burn out (smoke). When this happens all analog parts connected to the +/-15V can be damaged in a domino affect.