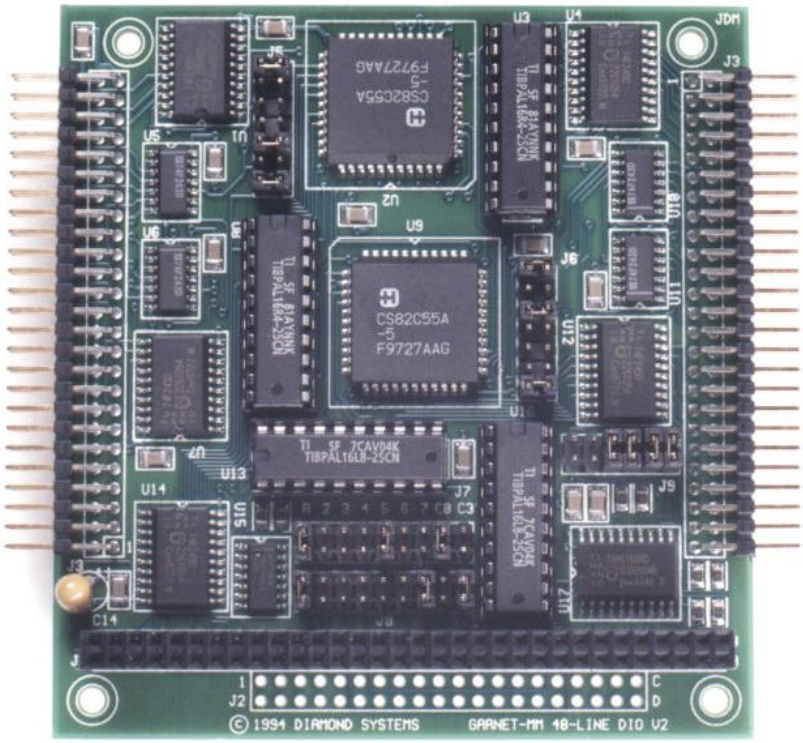
DIAMOND SYSTEMS CORPORATION

GARNET-MM

24- and 48-Line High-Current
Digital I/O PC/104 Module

User Manual V1.4



Diamond Systems Corporation
8430-D Central Ave.
Newark, CA 94560
Tel (510) 456-7800
Fax (510) 45-7878
techinfo@diamondsystems.com
www.diamondsystems.com

Table of Contents

1. DESCRIPTION

Garnet-MM is a PC/104 digital I/O board with either 24 or 48 lines of I/O. It contains one or two 82C55 ICs, each having 3 8-bit I/O ports. Each 82C55 has its own 50-pin I/O header for external connections. Direction on all ports is selected by programming control registers built in to the 82C55 chips. All I/O lines are buffered with transceivers, whose directions are controlled by logic which responds to the direction control values written to the 82C55s. Each line is capable of sinking 64mA in a logic low state or sourcing 15mA in a logic high state. The board requires only +5V for operation.

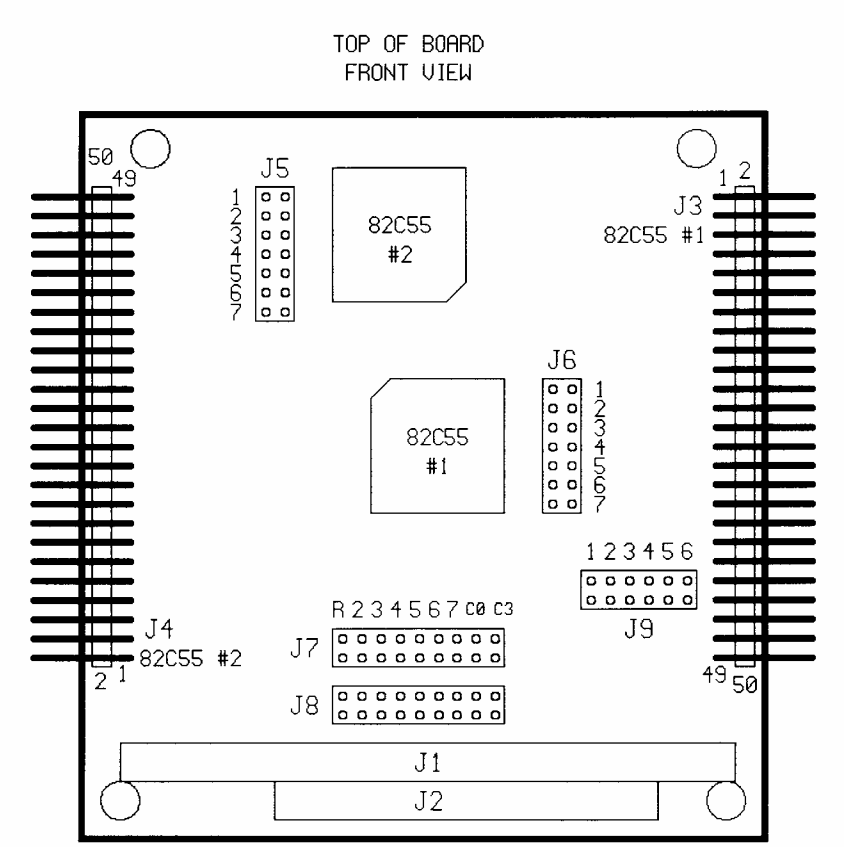
Garnet-MM's I/O headers are organized to allow direct interfacing to OPTO-22's isolated I/O racks, including the G4 series, the PB16-H, -J, -K, -L, PB8H, and the PB24HQ. These racks and I/O modules allow up to 3000 VRMS isolation between the computer and the user's signals. All control signals, power, and ground on the Garnet-MM I/O header match the corresponding signals on these I/O racks, so a single 50-pin ribbon cable, such as Diamond Systems' C50-18, is all that is needed to make the connection.

The board provides access to interrupt levels 2-7 on the PC bus for real-time background applications. Interrupts can be generated in two ways. In Mode 0 operation, a rising edge on one of four interrupt lines causes the board to generate an interrupt request on the bus. In Mode 1 operation, the 82C55 generates interrupts in response to handshake signals between Garnet-MM and external circuitry.

2. SPECIFICATIONS

Input voltage:	Low	0.0V min, +0.8V max
	High	2.0V min, 5.0V max
Output voltage:	Low	0.0V min, 0.55V max
	High	2.0V min, 4.7V max
Input current:	Low	-1.2mA max
	High	5uA max
Output current:	Low	64mA max at 0.55V max
	High	15mA max at 2.0V min
Ambient operating temperature:	0 - 70^{o}C	
Dimensions:	3.550" x 3.775" x 0.6"	
Power consumption:	+5V ±10% @ 160mA max quiescent, all outputs open	

6. GARNET-MM DRAWING



GARNET-MM HEADER LOCATION DIAGRAM

J1: PC/104 BUS 8-BIT HEADER
J2: PC/104 BUS 16-BIT EXTENSION HEADER (NOT INSTALLED)
J3: 82C55 #1 I/O HEADER
J4: 82C55 #2 I/O HEADER
J5: 82C55 #2 PORT C / MODE 1 CONFIGURATION
J6: 82C55 #1 PORT C / MODE 1 CONFIGURATION
J7: 82C55 #1 INTERRUPT CONFIGURATION
J8: 82C55 #2 INTERRUPT CONFIGURATION
J9: BASE ADDRESS SELECTION

3. I/O MAP

Garnet-MM occupies 8 bytes in I/O memory space:

Base +	Function	Direction	Notes
0	82C55 #1 Port A	Read/Write	
1	82C55 #1 Port B	Read/Write	
2	82C55 #1 Port C	Read/Write	
3	82C55 #1 Control	Write only	
4	82C55 #2 Port A	Read/Write	GMM-48 only
5	82C55 #2 Port B	Read/Write	GMM-48 only
6	82C55 #2 Port C	Read/Write	GMM-48 only
7	82C55 #2 Control	Write only	GMM-48 only

4. I/O HEADER PINOUT

Garnet-MM uses 50-pin I/O headers for the digital I/O. Header assignment is as follows:

Header	Location	Chip	I/O Addresses	Notes
J3	Right	82C55 #1	Base + 0 through Base + 3	
J4	Left	82C55 #2	Base + 4 through Base + 7	GMM-48 only

Note the pin 1 indication on each header; pin 1 on J3 is the upper left corner, while pin 1 on J4 is the lower right corner. J4 is upside down relative to the viewer but has the same orientation as J3 relative to the edge of the board.

Note: J4 is incorrectly marked J3 on some older boards.

A7	1	2	Ground
A6	3	4	Ground
A5	5	6	Ground
A4	7	8	Ground
A3	9	10	Ground
A2	11	12	Ground
A1	13	14	Ground
A0	15	16	Ground
C7	17	18	Ground
C6	19	20	Ground
C5	21	22	Ground
C4	23	24	Ground
C3	25	26	Ground
C2	27	28	Ground
C1	29	30	Ground
C0	31	32	Ground
B7	33	34	Ground
B6	35	36	Ground
B5	37	38	Ground
B4	39	40	Ground
B3	41	42	Ground
B2	43	44	Ground
B1	45	46	Ground
B0	47	48	Ground
+5	49	50	Ground

5. BOARD CONFIGURATION

Refer to the diagram on page 4 for positions of all headers referred to sections 5.1 and 5.2.

5.1. Base Address

Each board in the system must have a different base address. Garnet-MM's base address is set with header J9, located at the lower right corner of the board. Each of the six pairs of pins on J9 corresponds to a different address bit. A pair left open is equal to a 1, and a pair with a jumper installed is equal to a 0. The header is used to select address bits 9 - 4, resulting in an 16-byte I/O decode, of which only the lower 8 bytes are used (see I/O map on previous page). The leftmost pair selects address bit A9, and the rightmost pair selects address bit A4. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts. The table below lists recommended base address settings for Garnet-MM. The default setting is 300 Hex. "Open" means an open position, and "Inst" means a position with a jumper installed.

Base Address		**Header J9 Position**					
Hex	**Decimal**	**1**	**2**	**3**	**4**	**5**	**6**
220	544	Open	Inst	Inst	Inst	Open	Inst
240	576	Open	Inst	Inst	Open	Inst	Inst
250	592	Open	Inst	Inst	Open	Inst	Open
260	608	Open	Inst	Inst	Open	Open	Inst
280	640	Open	Inst	Open	Inst	Inst	Inst
290	656	Open	Inst	Open	Inst	Inst	Open
2A0	672	Open	Inst	Open	Inst	Open	Inst
2B0	688	Open	Inst	Open	Inst	Open	Open
2C0	704	Open	Inst	Open	Open	Inst	Inst
2D0	720	Open	Inst	Open	Open	Inst	Open
2E0	736	Open	Inst	Open	Open	Open	Inst
300	768 (Default)	Open	Open	Inst	Inst	Inst	Inst
330	816	Open	Open	Inst	Inst	Open	Open
340	832	Open	Open	Inst	Open	Inst	Inst
350	848	Open	Open	Inst	Open	Inst	Open
360	864	Open	Open	Inst	Open	Open	Inst
380	896	Open	Open	Open	Inst	Inst	Inst
390	912	Open	Open	Open	Inst	Inst	Open
3A0	928	Open	Open	Open	Inst	Open	Inst
3C0	960	Open	Open	Open	Open	Inst	Inst
3E0	992	Open	Open	Open	Open	Open	Inst

5.2. Interrupt Configuration

Most applications do not use the interrupt capability of Garnet-MM. If you are not using interrupts you can ignore this section.

Each 82C55 has its own independent interrupt circuit and configuration header. The two headers are located at the lower center of the board, just above the PC bus header. J7, the upper header, is used for chip #1 (Base + 0 through Base + 3), and J8, the lower header, is used for chip #2 (Base + 4 through Base + 7). Three jumpers are used in each header to configure the interrupt circuit.

The interrupt level is marked above each pair of pins. Install one jumper below the desired interrupt level. If interrupt are not desired, this jumper may be removed.

Install a jumper on the pair of pins marked "R" to connect a 1K ohm pulldown resistor to the selected interrupt level in accordance with PC/104 specifications. Only one resistor should be connected to any given interrupt level within a single system. The interrupt circuit works by driving the interrupt line high during a request and tristating the driver upon reset, so the resistor is required to pull the line down to a logic 0.

Each interrupt line is driven by either bit C0 or C3 of each 82C55. The rightmost two pairs of pins on J7 and J8 select which bit will drive the interrupt line. Install a jumper in either the C0 or C3 position, but not both. When port C is in input mode under Mode 0 operation, the interrupt signals are driven directly by the external connections on the I/O headers. When Port C is in output mode under Mode 0 operation, the interrupt signals are driven by the 82C55. In Mode 1 operation, interrupt signals are always driven by the 82C55 as part of the handshaking sequence.

5.3. Interface to OPTO-22 Racks

Since the I/O header on Garnet-MM is identical to the pinout on the header on many OPTO-22 racks, connection is made just through a standard 50-pin ribbon cable. One consideration applies:

On the OPTO-22 rack, there is a pair of jumpers named "Pin 1" and "Pin 49". These jumpers are used to select the source of +5 power to the rack. Pin 1 on Garnet-MM is I/O line A7, and pin 49 is +5. Therefore, cut the Pin 1 jumper away, but leave the Pin 49 jumper in place to provide power to the rack from pin 49 of the header.

5.4. Port Direction Control

Port direction is programmed with the control register in each 82C55. See the datasheet at the back of this manual for details. Two PALs on Garnet-MM (U3 and U8) respond to the control byte written and automatically set the port transceivers to the correct orientation.

7. MODE 1 OPERATION

Mode 1 on the 82C55 provides handshaking capabilities between the board and external equipment. Most applications do not use this feature. If you are doing “standard” digital I/O then you can skip this section.

In Mode 1, interrupts are generated by the 82C55 during the I/O process. Either bit C3 or bit C0 is used as the interrupt signal, depending on the configuration as described above. In Mode 1, the direction of these signals does not depend on the direction programmed in the 82C55 control register, so these signals must be rerouted to different positions in order to not interfere with the port transceivers. Two headers, J5 and J6, are provided for this purpose, and their use is described below. Because of this rerouting, the strobe and acknowledge signals listed below differ from the assignments shown in the 82C55 datasheet.

Input Operation: Port A and/or B is used for data input. A strobe signal is pulsed low to latch data into the 82C55. Both an acknowledge signal (Input Buffer Full) and the interrupt source pin go high in response. Reading from the 82C55 resets the two signals, readying the 82C55 for the next data value. Either or both strobe signals may be used, depending on whether the data is 8 or 16 bits.

Input, 82C55 #1	**Port A**	**Port B**
Strobe signal input:	1PC4 (J3 pin 23)	1PC5 (J3 pin 21)
Input buffer full output:	1PC2 (J3 pin 27)	1PC1 (J3 pin 29)
Interrupt signal:	1PC3	1PC0
Jumper configuration:	J6: 1, 4, 6	J6: 1, 4, 6
Rerouted bits:	1PC5 -> 1PC2	1PC5 -> 1PC2
	1PC2 -> 1PC5	1PC2 -> 1PC5

Input, 82C55 #2	**Port A**	**Port B**
Strobe input:	2PC4 (J4 pin 23)	2PC5 (J4 pin 21)
Input buffer full output:	2PC2 (J4 pin 27)	2PC1 (J4 pin 29)
Interrupt signal:	2PC3	2PC0
Jumper configuration:	J5: 2, 4, 7	J5: 2, 4, 7
Rerouted bits:	2PC5 -> 2PC2	2PC5 -> 2PC2
	2PC2 -> 2PC5	2PC2 -> 2PC5

Output Operation: Port A and/or Port B can be used for output. Each time a value is written to the 82C55, the value appears at the port's outputs, the interrupt signal goes low, and the Output Buffer Full signal goes low. Upon acquiring the new data, the external device pulses the Acknowledge signal low, causing the 82C55 to set the Output Buffer Full signal high and generate an interrupt request. The PC responds by writing a new value to the 82C55, resetting the Output Buffer Full and interrupt request signals. In Mode 1 output operation, the first data value is output prior to the first handshake operation. This means that if interrupts are being used with Mode 1 output, the first interrupt is generated immediately.

Output, 82C55 #1	**Port A**	**Port B**
Output buffer full output:	1PC2 (J3 pin 27)	1PC1 (J3 pin 29)
Acknowledge input:	1PC6 (J3 pin 19)	1PC7 (J3 pin 17)
Interrupt signal:	1PC3	1PC0
Jumper configuration:	J6: 2, 3, 5	J6: 2, 3, 5
Rerouted bits:	1PC7 -> 1PC2	1PC7 -> 1PC2
	1PC2 -> 1PC7	1PC2 -> 1PC7

Output, 82C55 #2	**Port A**	**Port B**
Output buffer full output:	2PC2 (J4 pin 27)	2PC1 (J4 pin 29)
Acknowledge input:	2PC6 (J4 pin 19)	2PC7 (J4 pin 17)
Interrupt signal:	2PC3	2PC0
Jumper configuration:	J5: 3, 5, 6	J5: 3, 5, 6
Rerouted bits:	2PC7 -> 2PC2	2PC7 -> 1PC2
	2PC2 -> 2PC7	2PC2 -> 1PC7

8. CONFIGURATION HEADER INFORMATION

J9: Base Address Select

Position	Function	Open	Jumper
1	Address bit A9	1	0
2	Address bit A8	1	0
3	Address bit A7	1	0
4	Address bit A6	1	0
5	Address bit A5	1	0
6	Address bit A4	1	0

Note: Base address bits 3 - 0 are always 0, meaning that valid base addresses are always on 16-byte boundaries. Position 1 is on the left; position 6 is on the right, nearest the label J9.

If you are not using interrupts or 82C55 mode 1, you can skip J5 – J8 configuration. J5 and J6 are factory-configured for Mode 0 operation.

J5: Port 2C Interrupt and Bit Mapping Configuration

Position	Mode 0	Mode 1 Input	Mode 1 Output
1	Jumper	Open	Open
2	Open	Jumper	Open
3	Open	Open	Jumper
4	Open	Jumper	Open
5	Jumper	Open	Jumper
6	Open	Open	Jumper
7	Jumper	Jumper	Open

Note: Position 1 is at the top of the header, nearest the label J5.

J6: Port 1C Interrupt and Bit Mapping Configuration

Position	Mode 0	Mode 1 Input	Mode 1 Output
1	Jumper	Jumper	Open
2	Open	Open	Jumper
3	Jumper	Open	Jumper
4	Open	Jumper	Open
5	Open	Open	Jumper
6	Open	Jumper	Open
7	Jumper	Open	Open

Note: Position 1 is at the top of the header, nearest the label J6.

J7: 82C55 #1 Interrupt Level Select

J8: 82C55 #2 Interrupt Level Select

Position	Function	Open	Jumper
2	IRQ2	Install only one jumper in	
3	IRQ3	any of these 6 locations	
4	IRQ4	to select the interrupt level	
5	IRQ5		
6	IRQ6		
7	IRQ7		
R	Pulldown resistor	No pulldown	Pulldown (max 1 per level)
C0	Interrupt source	Install only one jumper in either of these two	
C3		locations to select the interrupt source	

82C55A

CMOS Programmable Peripheral Interface

June 1998

Features

- **Pin Compatible with NMOS 8255A**
- **24 Programmable I/O Pins**
- **Fully TTL Compatible**
- **High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88**
- **Direct Bit Set/Reset Capability**
- **Enhanced Control Word Read Capability**
- **L7 Process**
- **2.5mA Drive Capability on All I/O Ports**
- **Low Standby Power (ICCSB) 10μA**

Ordering Information

PART NUMBERS		PACKAGE	TEMPERATURE RANGE	PKG. NO.
5MHz	8MHz			
CP82C55A-5	CP82C55A	40 Ld PDIP	0^oC to 70^oC	E40.6
IP82C55A-5	IP82C55A		-40^oC to 85^oC	E40.6
CS82C55A-5	CS82C55A	44 Ld PLCC	0^oC to 70^oC	N44.65
IS82C55A-5	IS82C55A		-40^oC to 85^oC	N44.65
CD82C55A-5	CD82C55A	40 Ld CERDIP	0^oC to 70^oC	F40.6
ID82C55A-5	ID82C55A		-40^oC to 85^oC	F40.6
MD82C55A-5/B	MD82C55A/B		-55^oC to 125^oC	F40.6
8406601QA	8406602QA	SMD#		F40.6
MR82C55A-5/B	MR82C55A/B	44 Pad CLCC	-55^oC to 125^oC	J44.A
8406601XA	8406602XA	SMD#		J44.A

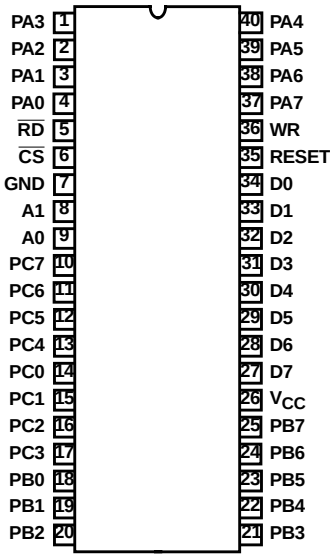
Description

The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

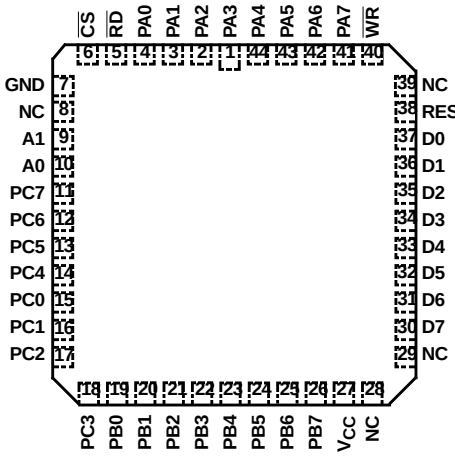
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Pinouts

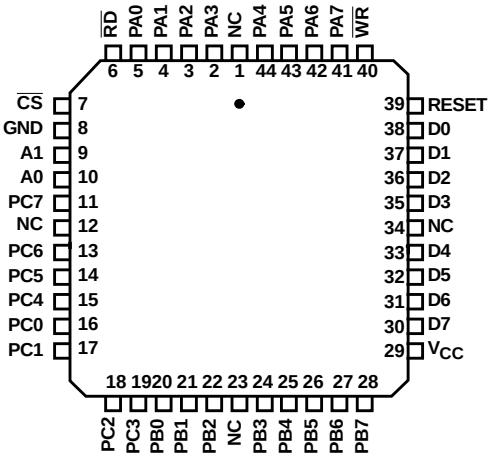
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW

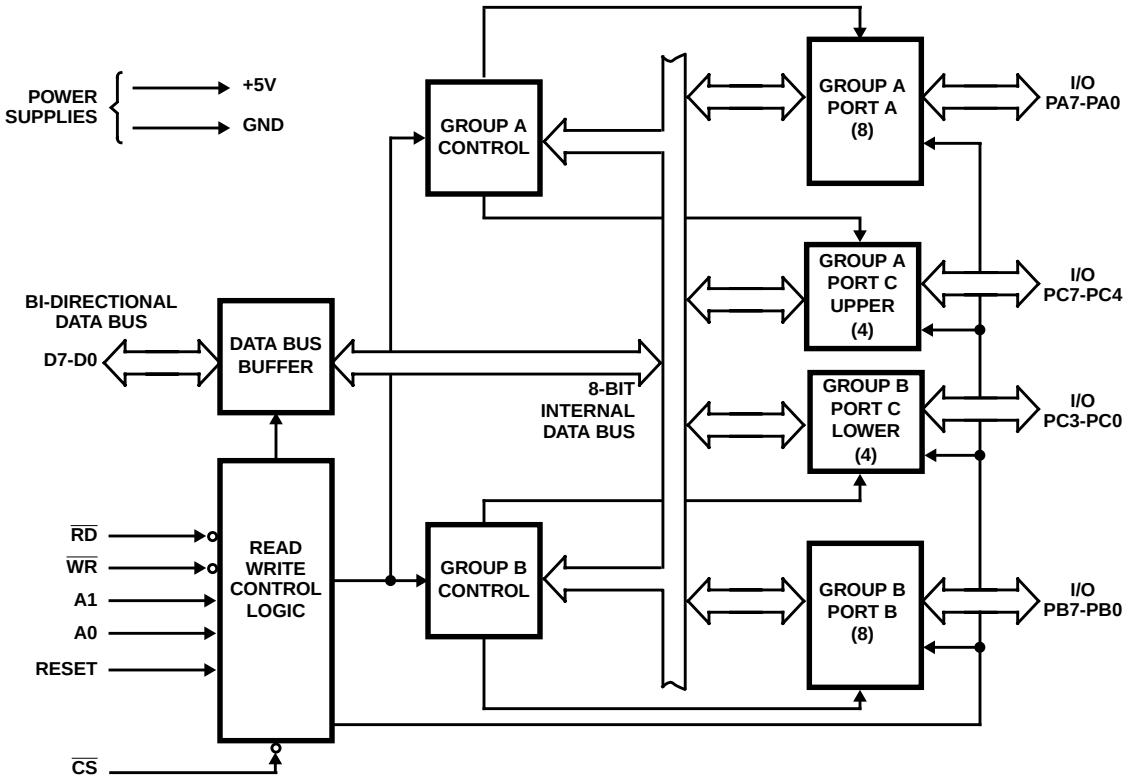


File Number **2969.2**

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the “Bus Hold” circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram



Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A “low” on this input pin enables the communcation between the 82C55A and the CPU.

(RD) Read. A “low” on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to “read from” the 82C55A.

(WR) Write. A “low” on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

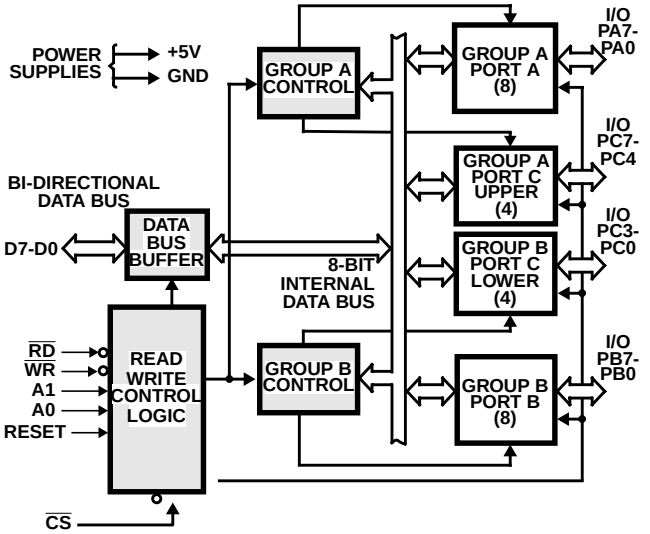


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A “high” on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. “Bus hold” devices internal to the 82C55A will hold the I/O port inputs to a logic “1” state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the 82C55A. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the “Basic Operation” table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

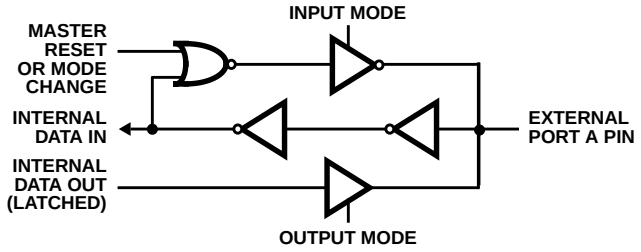


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

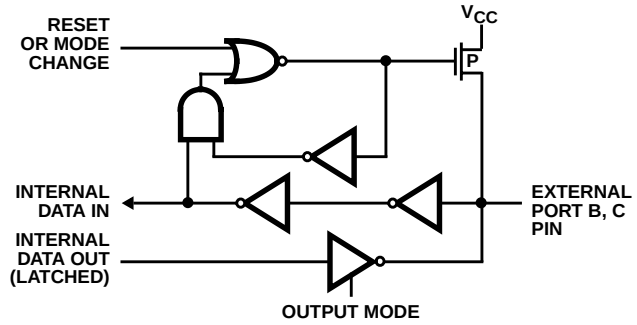


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

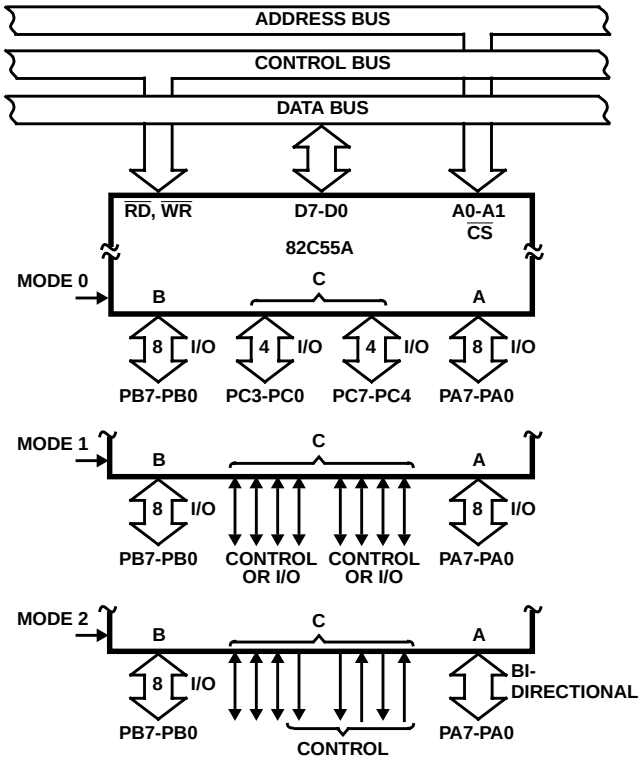


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

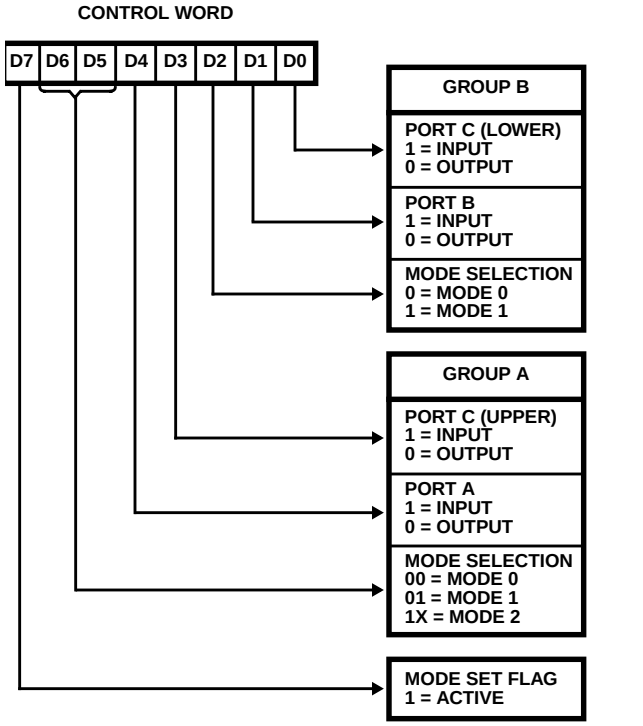


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be “tailored” to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

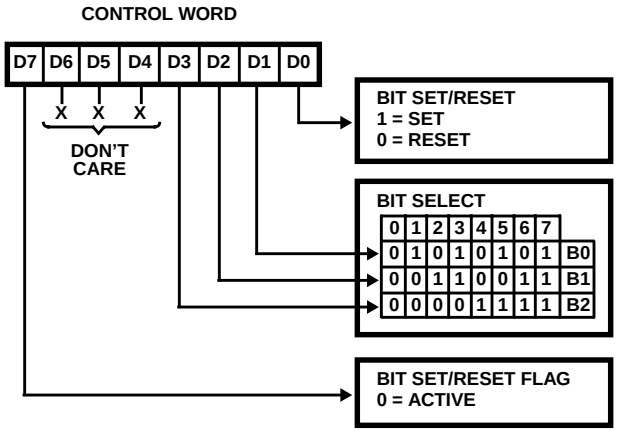


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

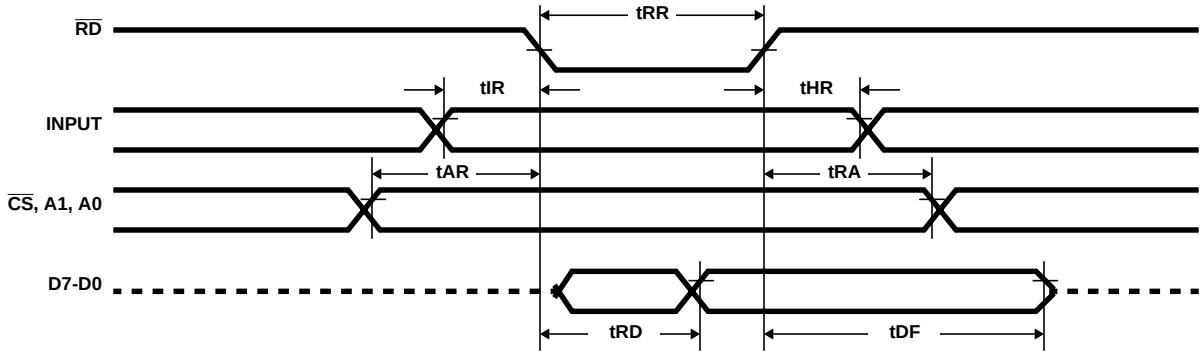
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

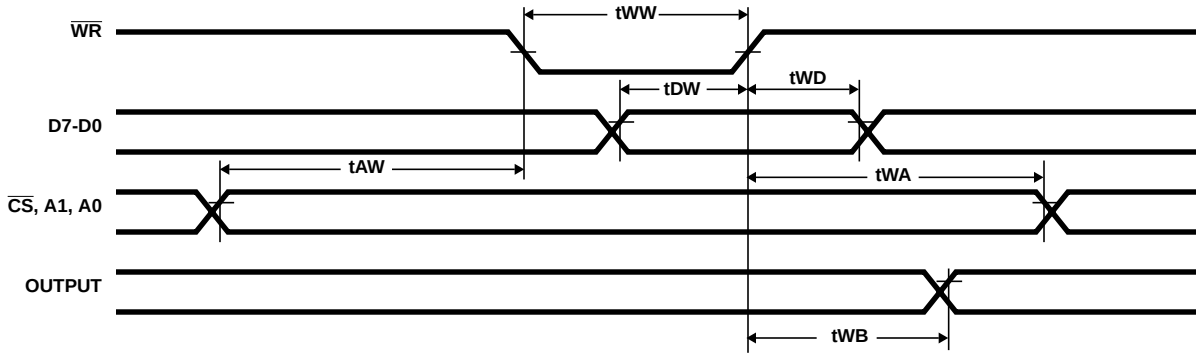
MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 (Basic Input)



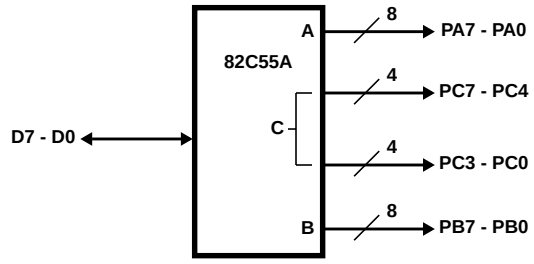
Mode 0 (Basic Output)



Mode 0 Configurations

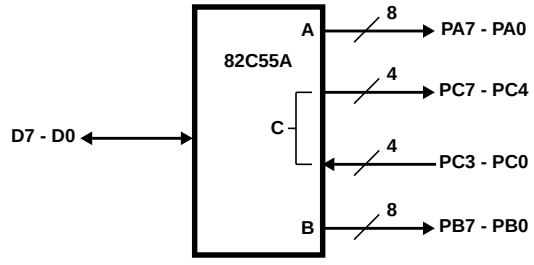
CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0



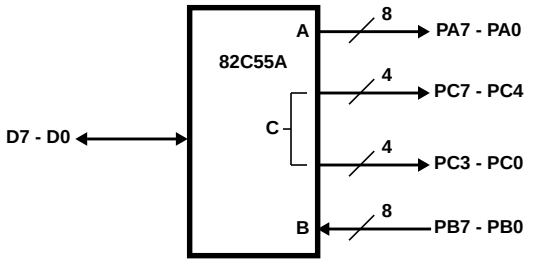
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1



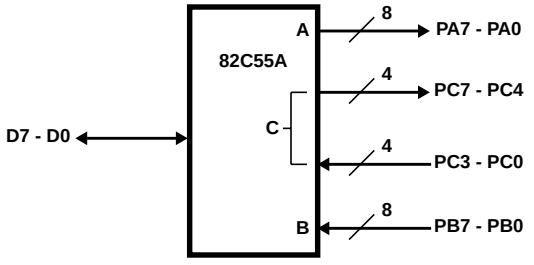
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0



CONTROL WORD #3

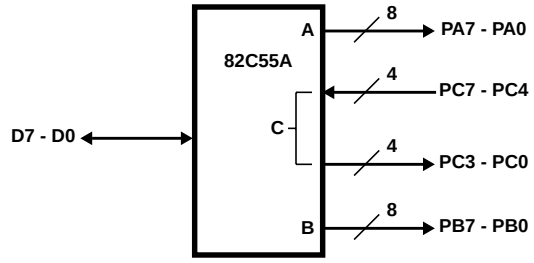
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1



Mode 0 Configurations (Continued)

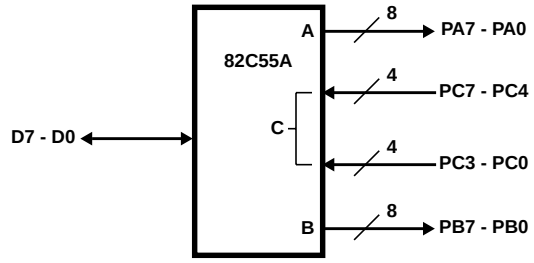
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



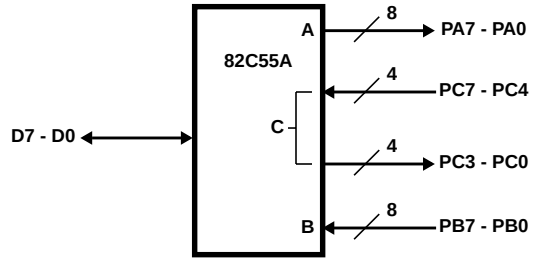
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1



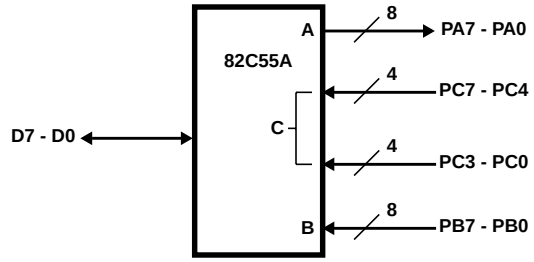
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



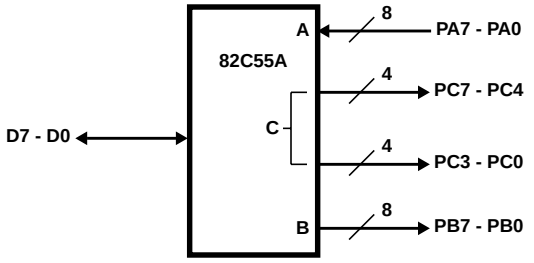
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



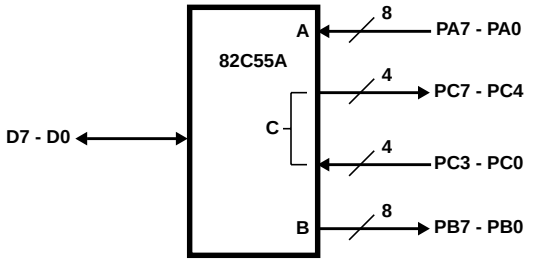
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



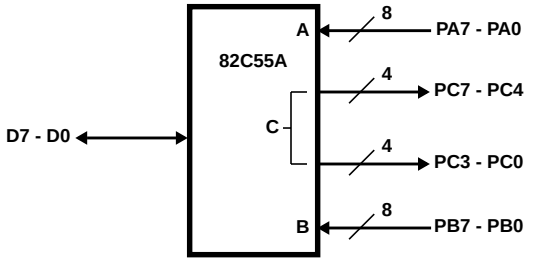
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



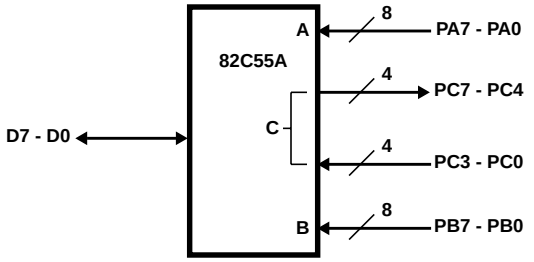
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



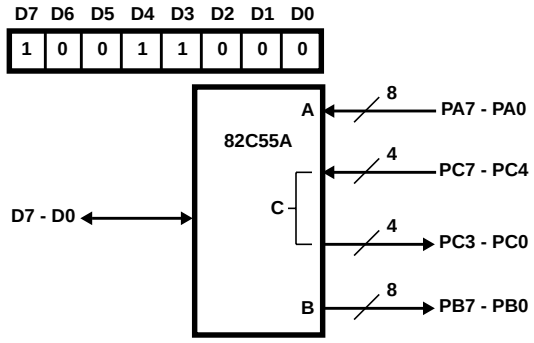
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

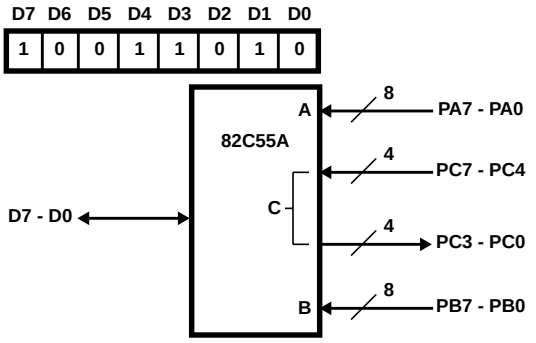


Mode 0 Configurations (Continued)

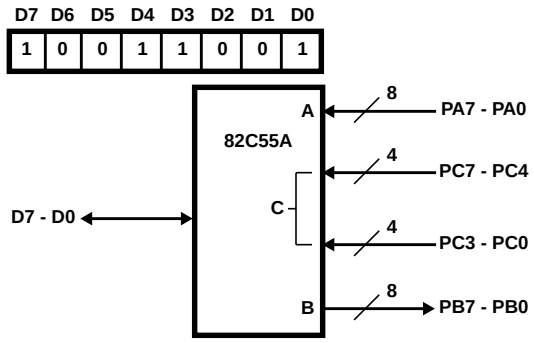
CONTROL WORD #12



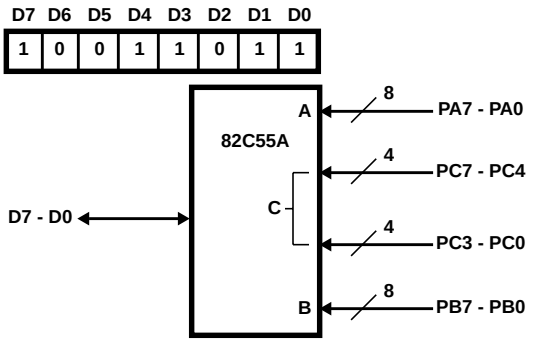
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or “hand shaking” signals. In mode 1, port A and port B use the lines on port C to generate or accept these “hand shaking” signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A “low” on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A “high” on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

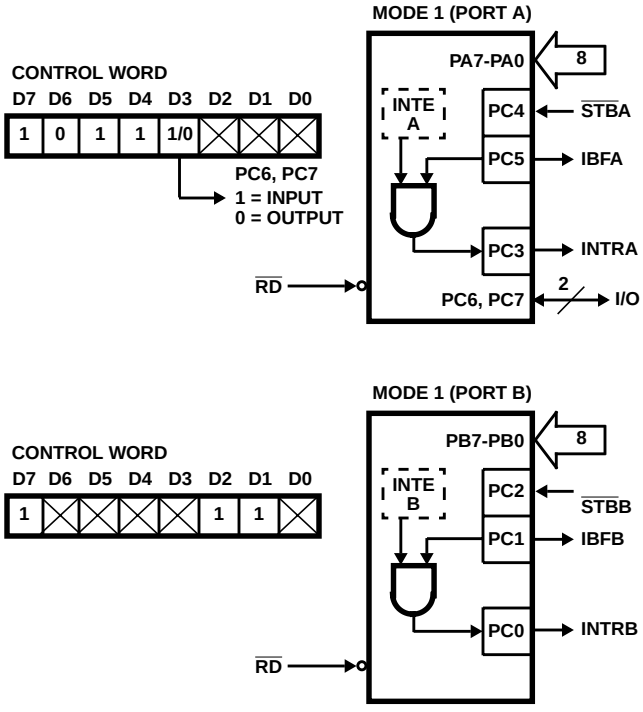


FIGURE 6. MODE 1 INPUT

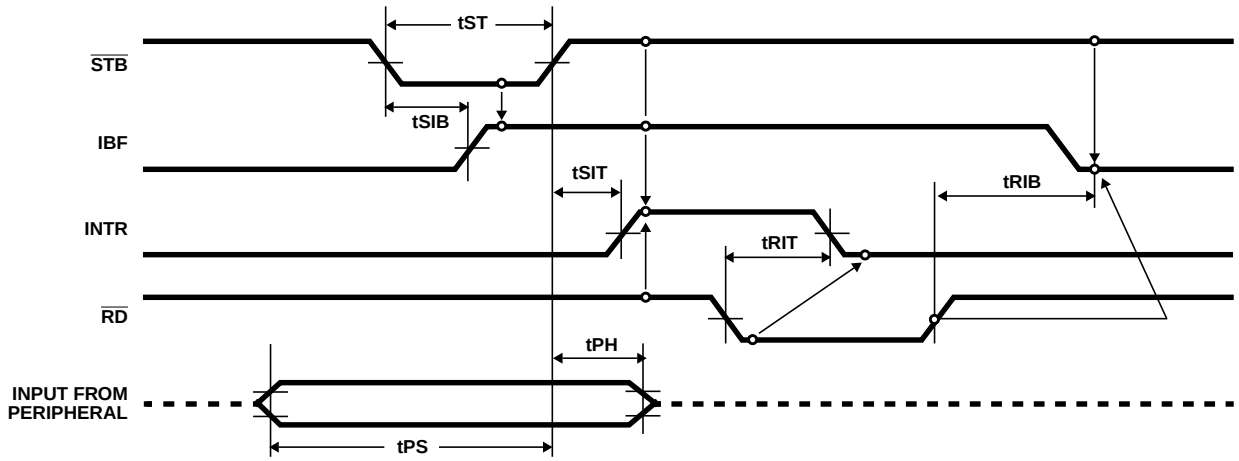


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A “high” on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go “low” to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$, (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A “low” on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

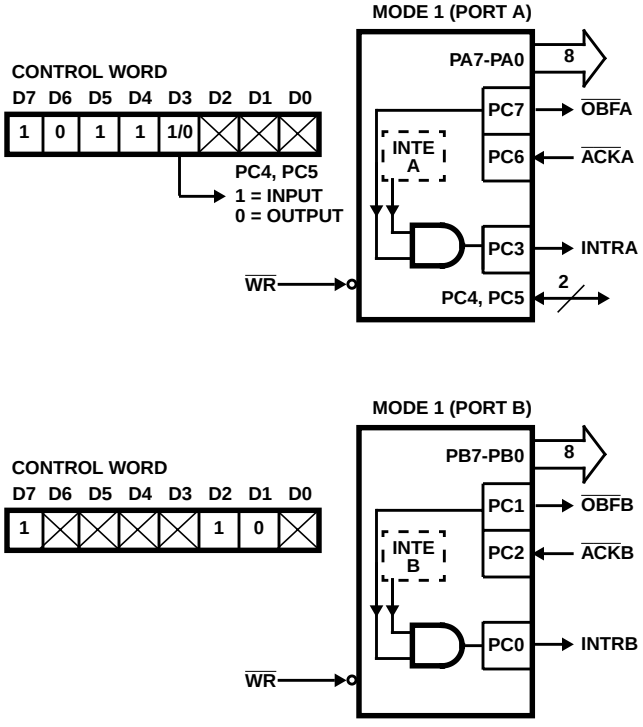


FIGURE 8. MODE 1 OUTPUT

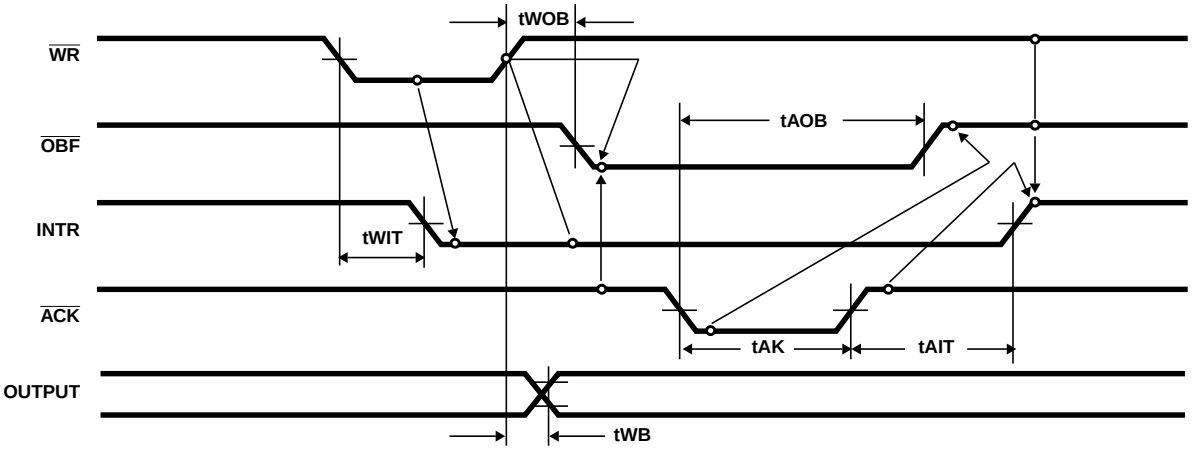
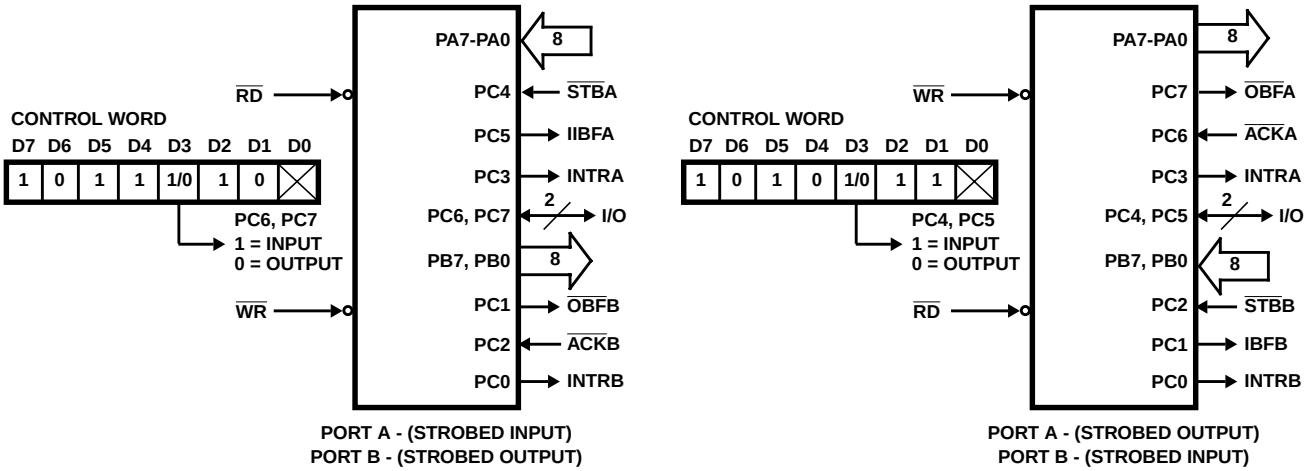


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). “Hand shaking” signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{\text{OBF}}$ - (Output Buffer Full). The $\overline{\text{OBF}}$ output will go “low” to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ - (Acknowledge). A “low” on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{\text{OBF}}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{\text{STB}}$ - (Strobe Input). A “low” on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A “high” on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

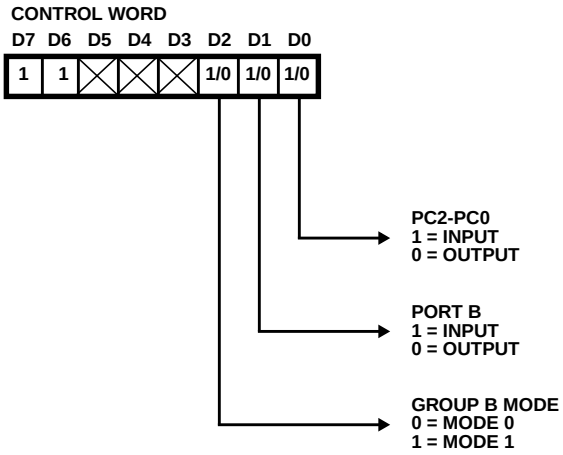


FIGURE 11. MODE CONTROL WORD

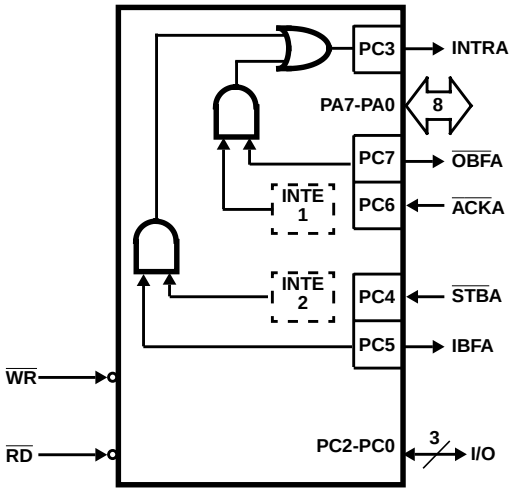
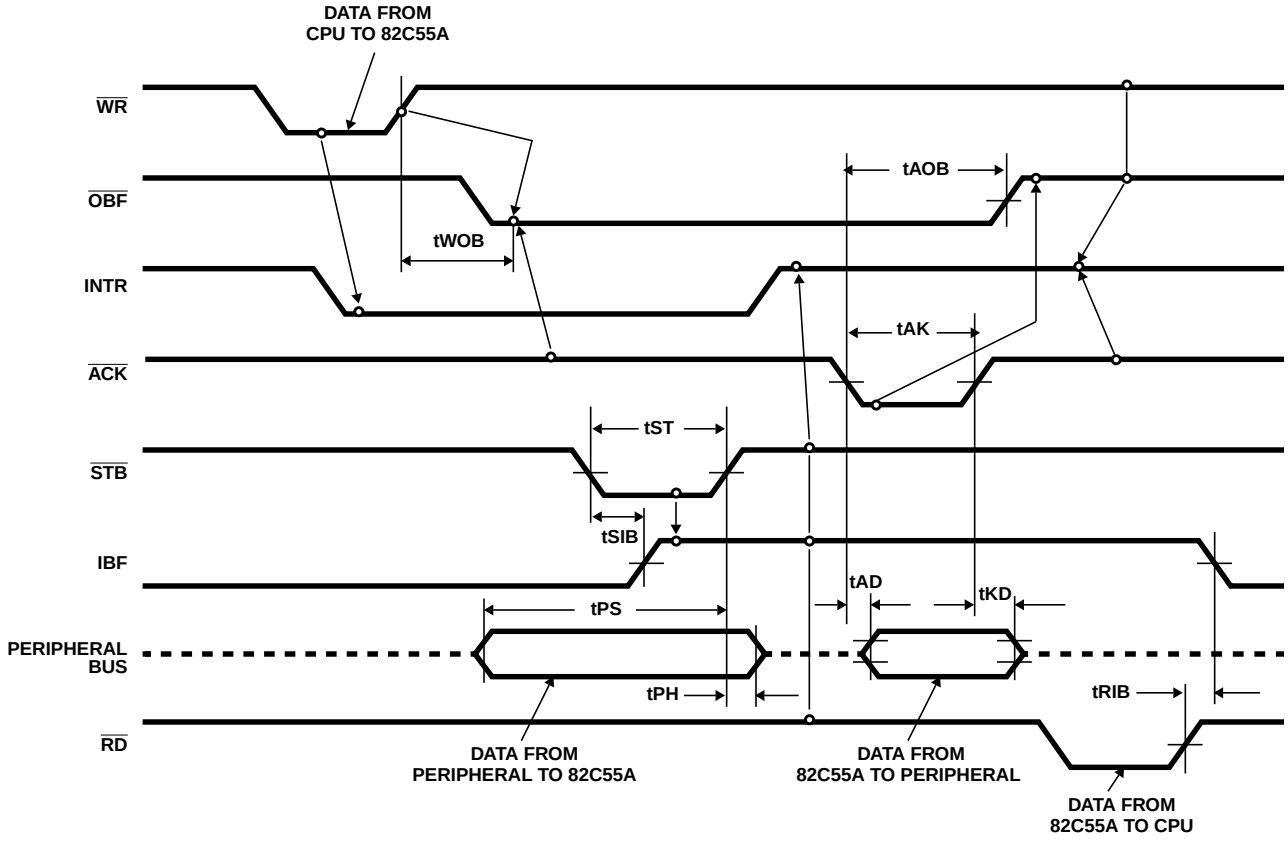


FIGURE 12. MODE 2



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ ÷ $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

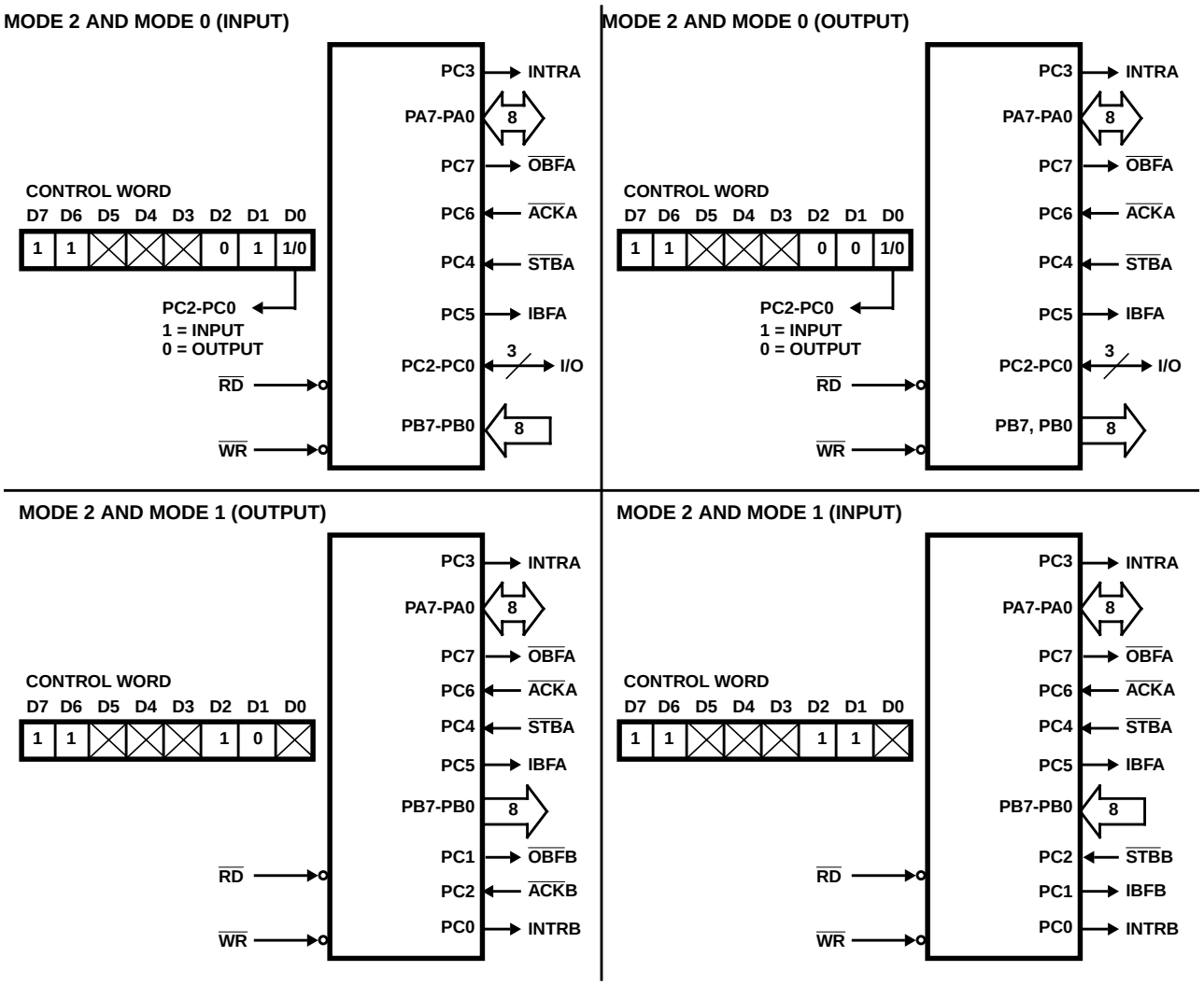


FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	↔	
PA1	In	Out	In	Out	↔	
PA2	In	Out	In	Out	↔	
PA3	In	Out	In	Out	↔	
PA4	In	Out	In	Out	↔	
PA5	In	Out	In	Out	↔	
PA6	In	Out	In	Out	↔	
PA7	In	Out	In	Out	↔	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	$\overline{OBF}$B	I/O	
PC2	In	Out	$\overline{STB}$B	$\overline{ACK}$B	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	$\overline{STB}$A	I/O	$\overline{STB}$A	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	$\overline{ACK}$A	$\overline{ACK}$A	
PC7	In	Out	I/O	$\overline{OBF}$A	$\overline{OBF}$A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a “Set Mode” command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a “Write Port C” command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a “Write Port C” command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the “Set/Reset Port C Bit” command must be used.

With a “Set/Reset Port Cea Bit” command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a “Set/Reset Port C Bit” command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the “Set Reset Port C Bit” command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts “hand shaking” signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the “status” of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or $\overline{STB}$B (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a “service routine” associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly “fit” the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

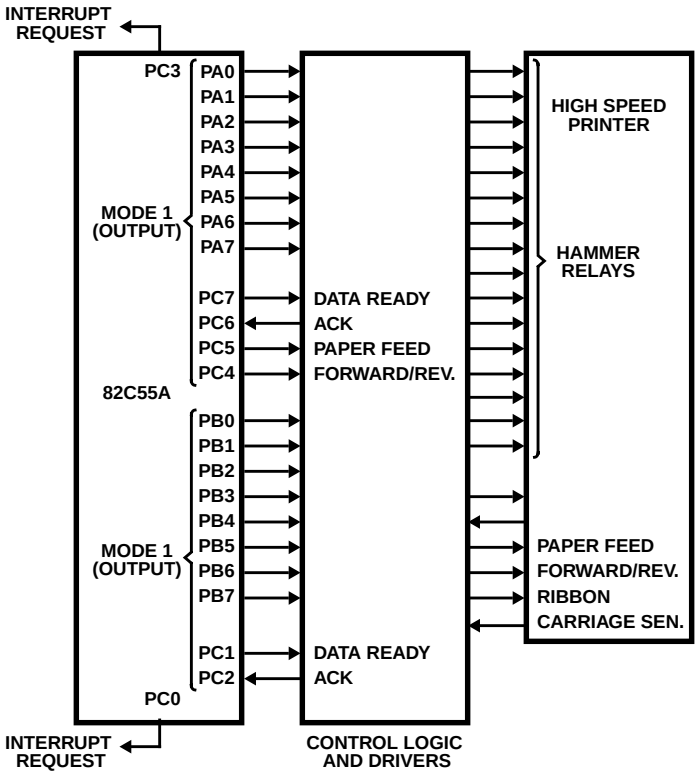


FIGURE 18. PRINTER INTERFACE